MT6139 Data Sheet

Table of contents

1 Introduction

1.1 Features

- **Receiver**
  - Direct conversion architecture
  - Quad differential input LNAs
  - Quadrature RF mixers
  - Fully integrated channel filter
  - 92 dB gain with 60 dB gain control range
- **Transmitter**
  - High precision IQ modulator
  - Direct conversion architecture
- **Frequency Synthesizer**
  - Single integrated, fully programmable fractional-N synthesizer
  - Fully integrated wide range RFVCO
  - Fast settling time suitable for multi-slot GPRS application
- **Voltage Control Crystal Oscillator (VCXO)**
  - 26 MHz crystal oscillator
  - Programmable capacitor array for coarse tuning
  - Internal varactor for fine tuning
- **Regulators**
  - Built-in low-noise, low-dropout (LDO) regulators for low-voltage VCO core
  - Built-in low-noise, low-dropout (LDO) regulators for VCXO core
  - Built-in LDO regulator for Sigma-Delta modulator
- **Low power consumption**
- **QFN (Quad Flat Non-lead) Package 40pin SMD**
- **3-wire serial interface**
- **MT6139 is fabricated using a 0.35 µm BiCMOS process**

1.2 Applications

GSM900 / DCS1800 dual-band handsets
GSM900 / PCS1900 dual-band handsets
GSM850 / PCS1900 dual -band handsets
GSM900 / DCS1800 / PCS1900 triple-band handsets
GSM850 / GSM900 / DCS1800 / PCS1900 quad-band handsets

1.3 General Descriptions

MT6139 is a highly integrated RF transceiver IC for Global Systems for Mobile communication (GSM850, GSM900), Digital Cellular communication Systems (DCS1800), and Personal Communication Services (PCS1900) quad band cellular systems. The MT6139 includes four LNA's, two RF quadrature mixers, a channel filter, a programmable gain amplifier for the receiver, a high precision IQ modulator for the transmitter, a VCXO oscillator, on-chip regulators, and a fully programmable sigma-delta fractional-N synthesizer with an on-chip LC VCO. The MT6139 includes control circuits to implement different operating modes. The device is housed in a 40-pin QFN SMD package with a downset paddle for additional grounding.

A functional block diagram of the MT6139 and its pin assignment is shown in Figure 1 .

1.4 Functional Block Diagram

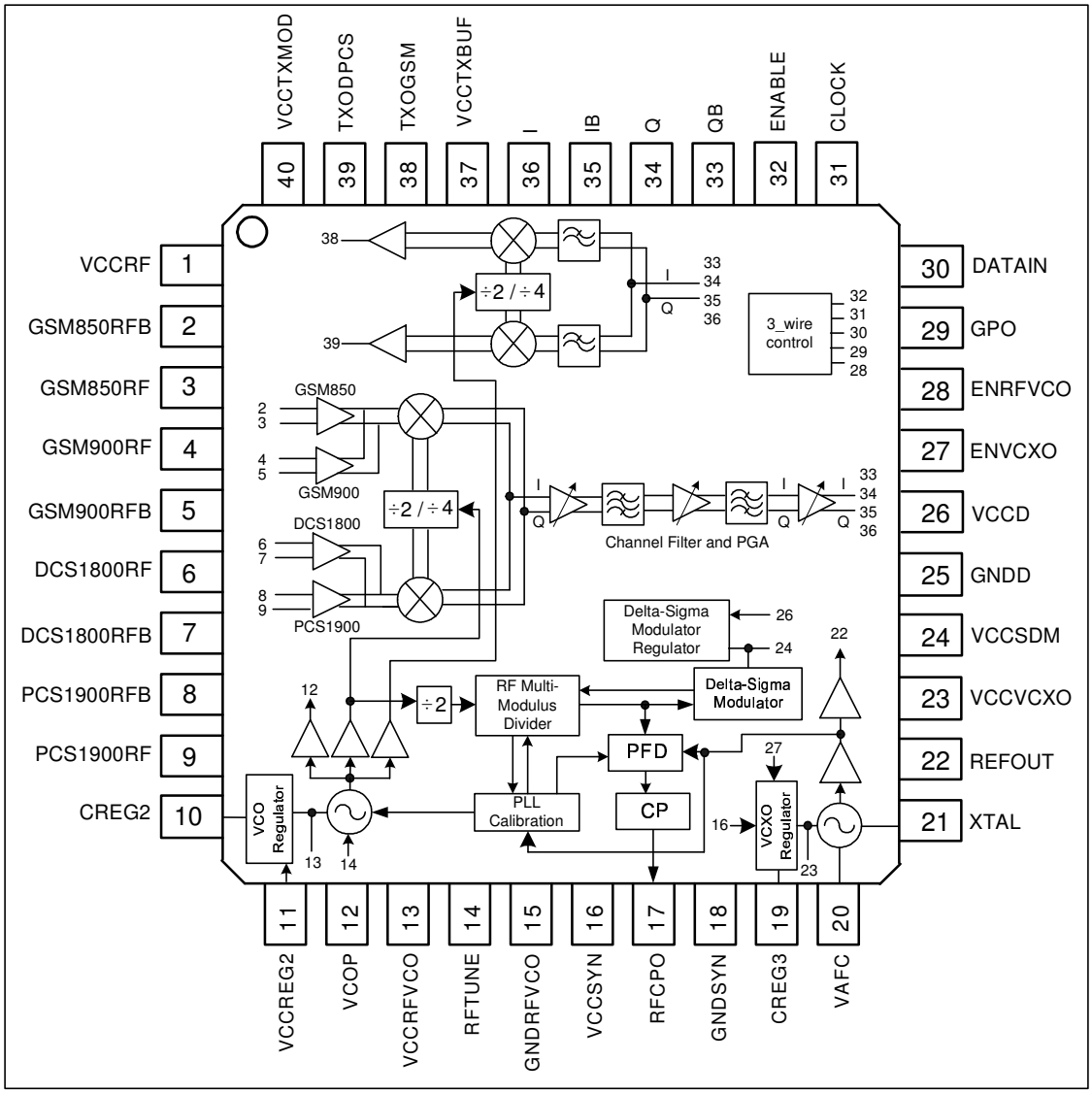


Figure 1 MT6139 Function Block Diagram

1.5 Pin Assignment and Description

Pin No.	Pin Name	Description
1	VCCRF	Rx RF block supply voltage / Tx DIV block supply voltage
2	GSM850RFB	Receiver GSM850 RF differential negative input
3	GSM850RF	Receiver GSM850 RF differential positive input
4	GSM900RF	Receiver GSM900 RF differential positive input
5	GSM900RFB	Receiver GSM900 RF differential negative input
6	DCS1800RF	Receiver DCS1800 RF differential positive input
7	DCS1800RFB	Receiver DCS1800 RF differential negative input
8	PCS1900RFB	Receiver PCS1900 RF differential negative input
9	PCS1900RF	Receiver PCS1900 RF differential positive input
10	CREG2	Regulator 2 external noise bypass
11	VCCREG2	Regulator 2 (RFVCO), Rx DIV block, RFVCO buffer power supply voltage
12	VCOP	RFVCO test differential positive output
13	VCCRFVCO	RFVCO supply voltage
14	RFTUNE	RFVCO tune input
15	GNDRFVCO	RFVCO ground
16	VCCSYN	RF synthesizer, PFD and charge pump supply voltage
17	RFCPO	RF synthesizer charge pump output
18	GNDSYN	RF synthesizer, PFD and charge pump ground
19	CREG3	Regulator 3 (VCXO) external noise bypass
20	VAFC	VCXO tuning
21	XTAL	26 MHz crystal reference input
22	REFOUT	26 MHz reference output
23	VCCVCXO	VCXO supply voltage
24	VCCSDM	Synthesizer Sigma-Delta Modulator (SDM) supply voltage, Regulator 1 (SDM) output
25	GNDD	3-wire digital circuit and RF synthesizer Sigma-Delta modulator ground
26	VCCD	Supply voltage for 3-wire digital circuit and supply voltage for Regulator 1 (SDM)
27	ENVCXO	Regulator 3 enable input for VCXO
28	ENRFVCO	Regulator 2 enable input for RFVCO
29	GPO	General-purpose output. Auxiliary test output
30	DATAIN	3-wire serial bus data input
31	CLOCK	3-wire serial bus clock input
32	ENABLE	3-wire serial bus enable input
33	QB	Q path negative BaseBand (BB) input / output
34	Q	Q path positive baseband input / output
35	IB	I path negative baseband input / output
36	I	I path positive baseband input / output
37	VCCTXBUF	TX BUF block supply voltage
38	TXOGSM	TX buffer output for GSM850 / GSM900
39	TXODPCS	TX buffer output for DCS1800 / PCS1900
40	VCCTXMOD	TX modulator supply voltage

Table 1 MT6139 Pin Description

2 Functional Description

2.1 Receiver

The receiver includes quad-band Low Noise Amplifiers (LNAs), RF quadrature mixers, on-chip channel filters, Programmable Gain Amplifiers (PGAs), and DC Offset Calibration (DCOC) loops. With additional one-time factory AM calibration procedure in advance, the IIP2 of the MT6139 can reach at least 50 dBm for all bands. The fully integrated channel filter rejects interference, blocking signals, without any external components. The MT6139 includes four differential LNAs for GSM850 (869 MHz-894 MHz), GSM900 (925 MHz-960 MHz), DCS1800 (1805 MHz-1880 MHz) and PCS1900 (1930 MHz –1990 MHz). The differential inputs are matched to 200 Ω SAW filters using LC networks. The gain of the LNAs can be controlled either high or low for an additional 37 dB dynamic range control. Following the LNAs are the quadrature RF mixers that down-convert the RF signal to the IF frequency. No external components are needed at the output of the RF mixers.

The IF signal is then filtered and amplified through a channel filter and a PGA. The multi-stage PGA is implemented between filtering stages to control the gain of the receiver. With a 2 dB gain steps, a 60 dB dynamic range of the PGA ensures a proper signal level for BaseBand (BB) setting requirement.

2.2 Transmitter

The transmitter consists of BB I/Q filters, I/Q modulators, frequency dividers, and buffer amplifiers. BB I/Q signals are fed into the RC low pass filter to reduce the out-band noise. The I/Q modulator is responsible for translating the BB I/Q signal to the Tx output frequency. To avoid the pulling problem, the Tx carrier is generated by dividing the Local Oscillator (LO) frequency from the synthesizer. The frequency dividers consists of both divided-by-2 and divided-by-4 circuits for GSM850/GSM900 and DCS1800/PCS1900 applications, respectively. Buffer amplifiers are adopted to amplify the I/Q modulator output signal to the adequate level to fulfill PA input power requirement.

2.3 RF Frequency Synthesizer

2.3.1 Synthesizer System Description

The MT6139 includes a single RF synthesizer with a fully integrated RFVCO to generate the local oscillator signals for Rx and Tx. The PLL locks the RFVCO to a precise reference frequency at 26 MHz. In order to reduce the inherent spurs caused by the fractional-N synthesizer, a 3rd-order sigma-delta modulator with a dithering function is used to generate the division number N of the Prescaler. The Prescaler is composed of a divided-by-2 divider and a multi-modulus divider with the programmable division number ranging from 32 to 127. A conventional digital-type PFD with a charge pump is used for phase comparison in the PLL. By changing the output current of the charge pump, the phase detector gain can be programmed from 50/2π μA/rad to 400/2π μA/rad.

To reduce the acquisition time or to enable fast settling time - for multi-slot data services such as GPRS, a digital loop (calibration loop) along with a fast-acquisition system are implemented in the RF synthesizer. During RF synthesizer programming, the RFVCO is pre-set to the vicinity of the desired frequency by a digital calibration loop. After the calibration, a fast-acquisition system is utilized for a period of time to facilitate fast locking. Once the acquisition is done, the PLL reverts back to the normal operation mode.

2.3.2 Synthesizer Frequency Programming for Rx Mode

The frequency range of the RF synthesizer for Rx mode is

Rx mode	GSM850	3476 MHz ~ 3576 MHz
	GSM900	3700 MHz ~ 3840 MHz
	DCS1800	3610 MHz ~ 3760 MHz
	PCS1900	3860 MHz ~ 3980 MHz

And the division number N can be decided by the following procedure.

1. Calculate LO frequency f_{VCO} from Rx channel frequency f_{CH}
   $f_{VCO} = 4 * f_{CH}$ for GSM850 and GSM900
   $f_{VCO} = 2 * f_{CH}$ for DCS1800 and PCS1900
2. Calculate N_{int} and N_{frac}
   $N = N_{int} + N_{frac}/130 = (f_{VCO}/2) / 26M$ N_{int} and N_{frac} are integers
   $0 \le N_{frac} < 130$
3. Use the binary equivalents of N_{int} and N_{frac} to program registers CW1-N_INTEGER[1] and CW1-N_FRACTION[2].

2.3.3 Synthesizer Frequency Programming for Tx Mode

The frequency range of the RF synthesizer for Tx mode is

Tx mode	GSM850	3296 MHz ~ 3396 MHz
	GSM900	3520 MHz ~ 3660 MHz
	DCS1800	3420 MHz ~ 3570 MHz
	PCS1900	3700 MHz ~ 3820 MHz

And the division number N can be decided by the following procedure.

1. Calculate LO frequency f_{VCO} from Tx channel frequency f_{CH}
   $f_{VCO} = 4 * f_{CH}$ for GSM850 and GSM900
   $f_{VCO} = 2 * f_{CH}$ for DCS1800 and PCS1900
2. Calculate N_{int} and N_{frac}
   $N = N_{int} + N_{frac}/130 = (f_{VCO}/2) / 26M$ N_{int} and N_{frac} are integers
   $0 \le N_{frac} < 130$
3. Use the binary equivalents of N_{int} and N_{frac} to program registers CW1-N_INTEGER and CW1-N_FRACTION.

2.3.4 Digital Calibration Loop

The MT6139 uses a digital calibration technique to reduce the PLL settling time. Once the RF synthesizer is programmed through a 3-wire serial interface, the calibration loop is activated. The main function of the calibration loop

[1] Please refer to MT6139 3-wire setting programming guide.
[2] Please refer to MT6139 3-wire setting programming guide.

is to preset the RFVCO to the vicinity of the desired frequncy quickly and correctly, thus aiding the PLL to settle faster. Since a large portion of initial frequency error is dealt with by the integrated calibration loop, the overall locking time can be drastically confined within a small range, irrespective of the desired frequency.

2.3.5 Fast-Acquisition System

After the digital calibration loop presets the RFVCO, the RF synthesizer reverts to the PLL operation and a fast-acquisition system is activated. For faster settling, the charge pump current is set to a higher current than normal setting for a period of time. Generally, 20 µs or 60 µs is allowed.

2.4 Voltage Control Crystal Oscillator

Voltage Control Crystal Oscillator (VCXO) consists of an amplifier, a buffer, and a programmable capacitor array. The amplifier is designed to be in parallel resonance with a standard 26 MHz crystal. The buffer provides a typical 600 mV_{pp} voltage swing at 26 MHz. The capacitor array, with 0.047 pF to 3 pF in steps of 0.047 pF, is used to tune the fixed offsets due to crystal manufacturing variations. A internal varactor that provides fine tuning combines with the capacitor array.

2.5 Regulator

The MT6139 houses internal regulators to provide low noise, stable, temperature and process independent supply voltages to the critical blocks in the transceiver. There are three regulators in MT6139, which are fed to VCO core circuit, Sigma-Delta modulator, and VCXO circuit, respectively. The first regulator which has only one output is fed to the Sigma-Delta modulator. The output voltage level is 2.0 V. When the circuit is disabled, the output is 2.8 V rather than 0 V via the internal P-channel MOSFET pass transistor. The maximum output current is 20 mA in the regulator. The second regulator's output is fed to the VCO core circuit. The level is 1.3 V and the maximum output current is 30 mA. The last regulator's output is fed to the VCXO circuit. The output voltage level is 2.2 V and the maximum output current is 10 mA in the regulator.

An internal P-channel MOSFET pass transistor is used to achieve a low dropout (LDO) voltage of less than 150 mV in all regulators. Besides the one fed to sigma-Delta modulator, there is an external capacitor connected to the noise bypass pin to lower the output noise level of the regulator.

3 MT6139 Hardware Control Pin Descriptions

A description of MT6139 hardware control pins and their functionality are shown in the table below.

Name	Setting	Description
ENVCXO	0	Power off VCXO
	1	Power on VCXO
ENRFVCO	0	Power off RFVCO
	1	Power on RFVCO

Table 2 Hardware Control Pin Description

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Prolonged exposure to absolute maximum ratings may reduce device reliability. Functional operation at these maximum ratings is not implied.

Item	Symbol	Min.	Max.	Unit
Power supply voltage (VCCRF)	VCCRF	TBD	TBD	V
Power supply voltage (VCCREG2)	VCCREG2	TBD	TBD	V
Power supply voltage (VCCSYN)	VCCSYN	TBD	TBD	V
Power supply voltage (VCCD)	VCCD	TBD	TBD	V
Power supply voltage (VCCMOD)	VCCMOD	TBD	TBD	V
Power supply voltage (VCCTXDIV)	VCCTXDIV	TBD	TBD	V
Pin voltage	V_T	TBD	TBD	V
Maximum power dissipation	P_T		TBD	mW
Operating temperature	T_{opr}	-20	80	℃
Storage temperature	T_{stg}	-55	125	℃

Table 3 Absolute Maximum Ratings

4.2 Recommended Operating Range

Item	Symbol	Min.	Typ.	Max	Unit
Power supply voltage (VCCRF)	VCCRF	2.7	2.8	2.9	V
Power supply voltage (VCCREG2)	VCCREG2	2.7	2.8	2.9	V
Power supply voltage (VCCSYN)	VCCSYN	2.7	2.8	2.9	V
Power supply voltage (VCCD)	VCCD	2.7	2.8	2.9	V
Power supply voltage (VCCMOD)	VCCMOD	2.7	2.8	2.9	V
Power supply voltage (VCCTXDIV)	VCCTXDIV	2.7	2.8	2.9	V
Operating ambient temperature	T_{opr}	-20	25	75	℃

Table 4 Recommended Operating Range

4.3 DC Specifications

Recommended Operating condition unless otherwise specified.

Item	Mode	Test condition	Min.	Typ.	Max.	Unit
Power supply current (Rx)	ALL[3]			77		mA
Power supply current (Tx)	GSM850			77		mA
	GSM900			77		
	DCS1800			74		
	PCS1900			74		
Power supply current (Warm-up)	ALL	Including VCXO		39		mA
Power supply current (Standby)	ALL	3 regulators + internal RFVCO + VCXO		25		mA
Power supply current (VCXO)	ALL	Regulator 3 + VCXO		3.1		mA
Power saving mode supply current (Sleep)	ALL	ENVCXO = 0 V, SDATA = 0 V, CLOCK = 0 V, ENABLE = 0 V		1.0	10	µA
Serial data VH (CLOCK, SDATA, ENABLE)	ALL	VCCD = 2.8 V	2.5			V
Serial data VL (CLOCK, SDATA, ENABLE)	ALL	VCCD = 2.8 V			0.3	V
Control pin VH (ENVCXO)	ALL		2.5			V
Control pin VL (ENVCXO)	ALL				0.3	V
Control pin VH (ENRFVCO)	ALL		2.5			V
Control pin VL (ENRFVCO)	ALL				0.3	V
IQ common mode DC output voltage	ALL	Receiver output DC		1.35		V
IQ common mode DC input voltage	ALL	Transmitter input DC		1.3		V

Table 5 DC specification

[3] ALL mode is GSM850 / GSM900 / DCS1800 / PCS1900 band

5 Receiver specifications

5.1 Receiver AC Specifications

Recommended operating condition unless otherwise specified.

Item	Mode	Test condition	Min	Typ	Max	unit
Receiver input frequency	GSM850		869		894	MHz
	GSM900		925		960	MHz
	DCS1800		1805		1880	MHz
	PCS1900		1930		1990	MHz
Differential receiver max voltage gain	GSM850	LNA = high gain RF = 882 MHz PGA = 60 dB	90	92		dB
	GSM900	LNA = high gain RF = 940 MHz PGA = 60 dB	90	92		dB
	DCS1800	LNA = high gain RF = 1842 MHz PGA = 60 dB	90	92		dB
	PCS1900	LNA = high gain RF = 1960 MHz PGA = 60 dB	90	92		dB
LNA differential input impedance	GSM850	Zin, RF = 882 MHz Note 1		TBD		Ω
	GSM900	Zin, RF = 945 MHz Note 1		TBD		Ω
	DCS1800	Zin, RF = 1842 MHz Note 1		TBD		Ω
	PCS1900	Zin, RF = 1960 MHz Note 1		TBD		Ω
Front-end LNA gain difference	GSM850	LNA = high gain to low gain RF = 882 MHz	37	39	41	dB
	GSM900	LNA = high gain to low gain RF = 940 MHz	37	39	41	dB
	DCS1800	LNA = high gain to low gain RF = 1842 MHz	37	39	41	dB
	PCS1900	LNA = high gain to low gain RF = 1960 MHz	37	39	41	dB
Receiver gain variation over temperature	ALL	-20 to 70 degree All gain settings			3.5	dB
2^{nd} order input intercept point	GSM850		50	60		dBm
	GSM900		50	60		dBm
	DCS1800		50	60		dBm
	PCS1900		50	60		dBm

High gain 3rd order input intercept point	GSM850		-15	-13		dBm
	GSM900		-15	-13		dBm
	DCS1800		-15	-13		dBm
	PCS1900		-15	-13		dBm
Receiver noise figure	GSM850	LNA = high gain, Note 1		3.5	4.5	dB
	GSM900			3.5	4.5	dB
	DCS1800			4.5	6.5	dB
	PCS1900			4.5	6.5	dB
	GSM850	LNA = low gain PGA = 60 dB Note 1		35	37	dB
	GSM900			35	37	dB
	DCS1800			38	40	dB
	PCS1900			38	40	dB
Receiver S/N with 3 MHz blocker	GSM850	Blocker = –23 dBm. Noise power is calculated within 130 kHz BW.	7	8		dB
	GSM900		7	8		dB
	DCS1800		5	6		dB
	PCS1900		5	6		dB
Receiver image rejection ratio	GSM850	Note 1	30	35		dB
	GSM900		30	35		dB
	DCS1800		25	30		dB
	PCS1900		25	30		dB
Receiver channel response attenuation	135 kHz	@ +/-200 kHz offset		+17		dB
		@ +/-400 kHz offset		+47		dB
		@ +/-600 kHz offset		+65		dB
		@ +/-1.6 MHz offset		+107		dB
	150 kHz	@ +/-200 kHz offset		+13		dB
		@ +/-400 kHz offset		+42		dB
		@ +/-600 kHz offset		+60		dB
		@ +/-1.6 MHz offset		+102		dB
Receiver group delay variation	135 kHz	For all gain settings 0-67.7 kHz		0.4		us
	150 kHz	For all gain settings 0-67.7 kHz		0.3		
Receiver filtering 3-dB BW	135 kHz	For all gain settings	105		165	kHz
	150 kHz	For all gain settings	120		180	kHz
PGA gain linearity	ALL	In any 20 dB setting		0.5	1	dB
		For all gain settings		0.8	1.5	dB
PGA gain step	ALL		1.75	2	2.25	dB
PGA dynamic range	ALL	PGA = 0 dB to 60 dB	59	60		dB
Receiver dynamic range	ALL		92			dB
IQ maximum output swing	ALL	For all gain settings	2.0	2.2		V_{p-p}

IQ common mode output voltage	ALL	For all gain settings	1.25	1.35	1.45	V
Output static dc offset (after dc calibration)	ALL	For all gain settings			150	mV

Table 6 AC Specification of Receiver

Note 1: Please refer to the detail description about test setup and environment that is included in the MT6139 test procedure and item.

5.2 GSM850 Band LNA input 2-port S-parameter

Note: The S-parameter is measured by connecting RFIN pin as PORT1 and RFINB pin as PORT2.

Freq	magS11	angS11	magS12	angS12	magS21	angS21	magS22	angS22
900 MHz								
905 MHz								
910 MHz								
915 MHz								
920 MHz								
925 MHz								
930 MHz								
935 MHz								
940 MHz								
945 MHz								
950 MHz								
955 MHz								
960 MHz								
965 MHz								
970 MHz								
975 MHz								
980 MHz								
985 MHz								
990 MHz								
995 MHz								
1.0 GHz								

Table 7 GSM850 Band LNA input 2-port S-parameter

5.3 GSM900 Band LNA input 2-port S-parameter

Note: The S-parameter is measured by connecting RFIN pin as PORT1 and RFINB pin as PORT2.

Freq	magS11	angS11	magS12	angS12	magS21	angS21	magS22	angS22
900 MHz								
905 MHz								
910 MHz								
915 MHz								
920 MHz								
925 MHz								
930 MHz								
935 MHz								
940 MHz								
945 MHz								
950 MHz								
955 MHz								

960 MHz								
965 MHz								
970 MHz								
975 MHz								
980 MHz								
985 MHz								
990 MHz								
995 MHz								
1.0 GHz								

Table 8 GSM900 Band LNA input 2-port S-parameter

5.4 DCS1800 Band LNA input 2-port S-parameter

Freq	magS11	angS11	magS12	angS12	magS21	angS21	magS22	angS22
1800 MHz								
1805 MHz								
1810 MHz								
1815 MHz								
1820 MHz								
1825 MHz								
1830 MHz								
1835 MHz								
1840 MHz								
1845 MHz								
1850 MHz								
1855 MHz								
1860 MHz								
1865 MHz								
1870 MHz								
1875 MHz								
1880 MHz								
1885 MHz								
1890 MHz								
1895 MHz								
1900 MHz								

Table 9 DCS1800 Band LNA input 2-port S-parameter

5.5 PCS1900 Band LNA input 2-port S-parameter

Freq	magS11	angS11	magS12	angS12	magS21	angS21	magS22	angS22
1900 MHz								
1905 MHz								
1910 MHz								
1915 MHz								
1920 MHz								
1925 MHz								
1930 MHz								
1935 MHz								
1940 MHz								
1945 MHz								

1950 MHz								
1955 MHz								
1960 MHz								
1965 MHz								
1970 MHz								
1975 MHz								
1980 MHz								
1985 MHz								
1990 MHz								
1995 MHz								
2000 MHz								

Table 10 PCS1900 Band LNA input 2-port S-parameter

6 Transmitter specifications

6.1 AC Specifications

Recommended operating condition unless otherwise specified.

Item	Mode	Test Conditions	Min.	Typ.	Max.	Unit
Frequency (RF)	GSM850		824		849	MHz
	GSM900		880		915	MHz
	DCS1800		1710		1785	MHz
	PCS1900		1850		1910	MHz
Frequency (LO)	GSM850		3296		3396	MHz
	GSM900		3520		3660	MHz
	DCS1800		3420		3570	MHz
	PCS1900		3700		3820	MHz
Phase error	GSM850	RMS value, 200 kHz BW		1	1.5	degree
	GSM900	Peak value, 200 kHz BW		2.5	4	degree
	DCS1800	RMS value, 200 kHz BW		2	2.5	degree
	PCS1900	Peak value, 200 kHz BW		5	9	degree
Carrier suppression ratio	ALL	All '1' GMSK (Differential encode: off) (baseband frequency = 67.7 kHz) IQ input swing = 0.5 Vp-p IQ common mode input voltage = 1.3 V		-35		dBc
Side-band suppression ratio				-35		dBc
IM3				-45		dBc
Average modulation spectrum	ALL	200 kHz offset (30 kHz bandwidth)		-36	-33	dBc
	GSM850 GSM900	400 kHz offset (30 kHz bandwidth)		-68	-65	dBc
	DCS1800 PCS1900			-65	-63	
	ALL	600 kHz offset (30 kHz bandwidth)		-73	-70	dBc
	ALL	1.2 MHz to 1.8 MHz offset (30 kHz bandwidth)		-78	-75	dBc
	ALL	1.8 MHz to 3 MHz offset (100 kHz bandwidth)		-77	-74	dBc
	ALL	3 MHz to 6 MHz offset (100 kHz bandwidth)		-77		dBc

	ALL	6 MHz upward offset (100 kHz bandwidth)		-77		dBc
Tx noise in Rx band	GSM850	925 MHz to 935 MHz 10 MHz up from Tx band			-156	dBc/Hz
	GSM900	935 MHz to 960 MHz 20 MHz up from Tx band			-156	dBc/Hz
	DCS1800	1805 MHz to 1880 MHz 20 MHz up from Tx band			-152	dBc/Hz
	PCS1900	1930 MHz to 1990 MHz 20 MHz up from Tx band			-152	dBc/Hz
IQ input swing	ALL	Single ended	0.4	0.5	0.6	Vp-p
IQ common mode input voltage	ALL		1.0	1.3	1.4	V
Output power level	GSM850 GSM900	PA Driver Amplifier. R_{load} = 50 Ω	0	2	5	dBm
	DCS1800 PCS1900	PA Driver Amplifier. R_{load} = 50 Ω	1	3	6	dBm
Output harmonics	ALL	PA Driver Amplifier.			-30	dBc

Table 11 AC Specification of Transmitter

7 Frequency Synthesizer Specifications

7.1 Specifications

Recommended Operating condition unless otherwise specified.

Item	Mode	Test condition	Min.	Typ.	Max.	Unit
Power supply (VCCRFCP and VCCSYN)	ALL		2.6	2.8	3	V
Current consumption (ICCSYN)	ALL			9		mA
Current consumption (ICCRFCP)	ALL	CW0-SYNCP[4] = 00		1		mA
Frequency range	ALL		3200		4100	MHz
Reference frequency	ALL			26		MHz
Frequency step resolution	ALL			200		kHz
Phase detector gain	ALL	CW0-SYNCP = 00		50/2π		µA /rad
		CW0-SYNCP = 01		100/2π		
		CW0-SYNCP = 10		200/2π		
		CW0-SYNCP = 11		400/2π		
Phase detector sink versus source mismatch	ALL	V_{CPO} = VCCRFCP/2		5		%
Phase detector gain versus voltage	ALL	0.4 V < V_{CPO} < VCCRFCP – 0.4 V		10		%
In-band phase noise	ALL	@10 kHz offset		-74		dBc /Hz
Phase noise	ALL	@400 kHz offset			-111	dBc /Hz
		@3 MHz offset			-134	
Calibration time	ALL				32	µs
Spurious performance	GSM850 / GSM900 Rx	@200 kHz offset			-50	dBc
		@400 kHz offset			-50	
		@600 kHz offset			-70	
		@800 kHz offset			-60	
		@1 MHz offset			-80	
		@1.2 MHz offset			-70	
		@1.4 MHz offset			-80	
		@>3 MHz offset			-80	
	Tx	@1.6 MHz offset			-80	
		@>= 3 MHz offset			-80	
Lock time (t_{lock})	ALL	Frequency error < 2 kHz			200	µs
Frequency error of calibration loop	ALL		-5.5		5.5	MHz

[4] Please refer to the control word register descriptions of MT6139 3-wire setting programming guide

Varactor tuning voltage range (V_{tf})	ALL		1.0		1.6	V

Table 12 Specifications of RF Frequency Synthesizer

8 Specification for RFVCO and Buffer

Recommended Operating condition unless otherwise specified.

Item	Mode	Test condition	Min.	Typ.	Max.	Unit
Current consumption (VCO core only)	ALL	RX		19		mA
		TX		22		
Current consumption (buffers only)	ALL				19	mA
Power supply of VCO	Rx			1.23		V
	Tx			1.3		
Frequency range	GSM850	RX	3476		3576	MHz
	GSM900	RX	3684		3840	
	DCS1800	RX	3610		3760	
	PCS1900	RX	3860		3980	
	GSM850	TX	3296		3396	
	GSM900	TX	3504		3660	
	DCS1800	TX	3420		3570	
	PCS1900	TX	3700		3820	
Phase noise	ALL	@ 400 kHz offset			-111	dBc/Hz
		@ 600 kHz offset			-115	
		@ 3 MHz offset			-134	
Phase noise degradation for Ta = -20 ~ 80 ℃	ALL			± 3		dB
Frequency shift for Ta = -20 ~ 80 ℃	ALL		± 6		± 26	MHz
Tuning sensitivity (K_{vco}) @ Vtune = 1.2 V	ALL		18	31	45	MHz/V
K_{vco} variation for Vtune = 1.0 ~ 1.6 V	ALL	3296 MHz < f_{vco} < 3396 MHz	18		29	MHz/V
		3420 MHz < f_{vco} < 3660 MHz	19		34	
		3684 MHz < f_{vco} < 3840 MHz	23		40	
		3860 MHz < f_{vco} < 3980 MHz	27		45	
Tuning voltage at calibration state (frequency centering voltage)	ALL		1.18	1.2	1.22	V
Frequency step	ALL		6	14	26	MHz

Varactor covered frequency range (Vtune = 0.4 ~ 2.4 V)	ALL		40	56	92	MHz
Number of partitioned sub-band	ALL			64		
Subband coverage for single frequency	ALL		2			
The maximum oscillation frequency	ALL	Sub-band No.= 0 and Vtune = 2.4 V		4100		MHz
The minimum oscillation frequency	ALL	Sub-band No.= 127 and Vtune = 0.4 V		3140		MHz
Pulling figure (VSWR = 2:1 for all phase)	ALL				1	MHz
Pushing figure (VCCREG2 = 2.7 ~ 2.9 V)	ALL			TBD		MHz
Quadrature amplitude error	ALL				1	dB
Quadrature phase error	ALL				1.5	deg.
Output signal swing	ALL		200			mV_{pp}
Input impedance at port VCOP	ALL			213.55 + j44.66		Ohm

Table 13 Specification of RFVCO and Buffer

9 Voltage Control Crystal Oscillator (VCXO) Specifications

Recommended Operating condition unless otherwise specified.

Item	Test condition	Min.	Typ.	Max.	Unit
Supply current	VCCVCXO = 2.2 V		2.7		mA
Operating frequency	Crystal Cload = 12 pF / Res = 35 Ω max.		26		MHz
Output frequency	Baseband clock		26		MHz
Switched capacitor value	6 bits switch control from 0 to 63	0		3	pF
Switched capacitor step			0.047		pF
Varactor	Vbias = 0 V		10		pF
	Vbias = 3 V		5		pF
Negative resistance			TBD		Ω
Buffer output level	26 MHz baseband clock (Load = 37 - j610 Ω @ Frequency = 26 MHz)	400	600		mVpp
Duty cycle	26 MHz baseband clock	45		55	%
Buffer output 2nd harmonic	Load = 20 pF		-20	-5	dBc
Buffer output 3rd harmonic	Load = 20 pF		-10	-5	dBc
Start-up time	Including Regulator 3 power on time by ENVCXO pull high			5	ms

Table 14 Specification of VCXO

10 Regulator specifications

10.1 Regulator 1 (for Sigma-Delta modulator) specifications

V_{IN} = 2.8 V, Ta = 25 ℃, C_{out} = 2.2 µF

Item	Test condition	Min.	Typ.	Max.	Unit
Input voltage		2.7	2.8	2.9	V
Output voltage		1.9	2	2.1	V
Maximum output current			20		mA
Ground pin current	$I_{out,SDM}$ = 20 mA		218		µA
Dropout voltage	V_{in}-V_{out} when V_{out} = ($V_{out,\ nominal}$ - 100 mV), $I_{out,SDM}$ = 20 mA			500	mV
Line regulation	V_{in} = 2.7 V to 2.9 V, $I_{out,SDM}$ = 20 mA			1	mV
Load regulation	$I_{out,SDM}$ = 1 mA to 20 mA			1	mV
Power supply ripple rejection	f = 216.7 Hz, $I_{out,SDM}$ = 20 mA	40	50		dB
Temperature coefficient	V_{in} = 2.8 V, $I_{out,SDM}$ = 20 mA		80		ppm/℃
Output disable voltage	When circuit is disabled	2.6		2.9	V

Table 15 Specification of Regulator for Sigma-Delta Modulator

10.2 Regulator 2 (for RFVCO core) specifications

Ta = 25 ℃, C_{out} = 2.2 µF, C_{bp} = 0.1 µF

Item	Test condition	Min.	Typ.	Max.	Unit
Input voltage (VCCREG2)		2.7	2.8	2.9	V
Output voltage of VCO		1.25	1.3	1.35	V
Noise bypass terminal voltage			1.227		V
Maximum output current of VCO			30		mA
Ground pin current	$I_{out,VCO}$ = 30 mA		325		µA
Dropout voltage of VCO	V_{in}-V_{out} when V_{out} = ($V_{out,\ nominal}$ - 100 mV), $I_{out,VCO}$ = 30 mA		TBD		mV
Line regulation of VCO	V_{in} = 2.7 V to 2.9 V, $I_{out,VCO}$ = 30 mA			10	mV
Load regulation of VCO	$I_{out,VCO}$ = 1 mA to 30 mA			10	mV
Output voltage noise of VCO	f = 10 Hz to 100 kHz, C_{bp} = 0.1 µF, C_{out} = 2.2 µF		20	60	μV_{rms}
Power supply ripple rejection of VCO	f = 216.7 Hz, $I_{out,VCO}$ = 30 mA	50	60		dB
Temperature coefficient of VCO	V_{in} = 2.8 V, $I_{out,VCO}$ = 30 mA, TC = ΔV_{OUT}/[$V_{out,\ nominal}$*ΔT], ΔT = 80 - (-20) = 100 ℃		85		ppm/℃
Turn-on time of VCO	$V_{out,VCO}$ step from 0 to $V_{outVCO,\ nominal}$ ± 4 %, $C_{out,VCO}$ = 2.2 µF		30	40	µSec

Table 16 Specification of Regulator for RFVCO Core Circuit

10.3 Regulator 3 (for VCXO) specifications

Ta = 25 ℃, C_{out} = 2.2 µF, C_{bp} = 0.1 µF

Item	Test condition	Min.	Typ.	Max.	Unit
Input voltage (VCCVCXO)		2.7	2.8	2.9	V
Output voltage of VCXO		2.15	2.2	2.25	V
Noise bypass terminal voltage			1.227		V
Maximum output current of VCXO			5		mA
Ground pin current	$I_{out,VCXO}$ = 5 mA		325		µA
Dropout voltage of VCXO	V_{in}-V_{out} when V_{out} = ($V_{out,\ nominal}$ - 100 mV), $I_{out,VCXO}$ = 3 mA		TBD		mV
Line regulation of VCXO	V_{in} = 2.7 V to 2.9 V, $I_{out,VCXO}$ = 5 mA			10	mV
Load regulation of VCXO	$I_{out,VCXO}$ = 1 mA to 5 mA			10	mV
Output voltage noise of VCXO	f = 10 Hz to 100 kHz, C_{bp} = 0.1 µF, C_{out} = 2.2 µF		20	60	μV_{rms}
Power supply ripple rejection of VCXO	f = 216.7 Hz, $I_{out,VCXO}$ = 5 mA	50	60		dB
Temperature coefficient of VCXO	V_{in} = 2.8 V, $I_{out,VCXO}$ = 5 mA, TC = $\Delta V_{OUT}/[V_{out,\ nominal}*\Delta T]$, ΔT = 80 - (-20) = 100 ℃		85		ppm/℃
Turn-on time of VCXO	$V_{out,VCO}$ step from 0 to $V_{outVCO,\ nominal}$ ± 4 %, $C_{out,VCO}$ = 2.2 µF		20	40	µSec

Table 17 Specification of Regulator for VCXO Circuit

11 Package Dimensions

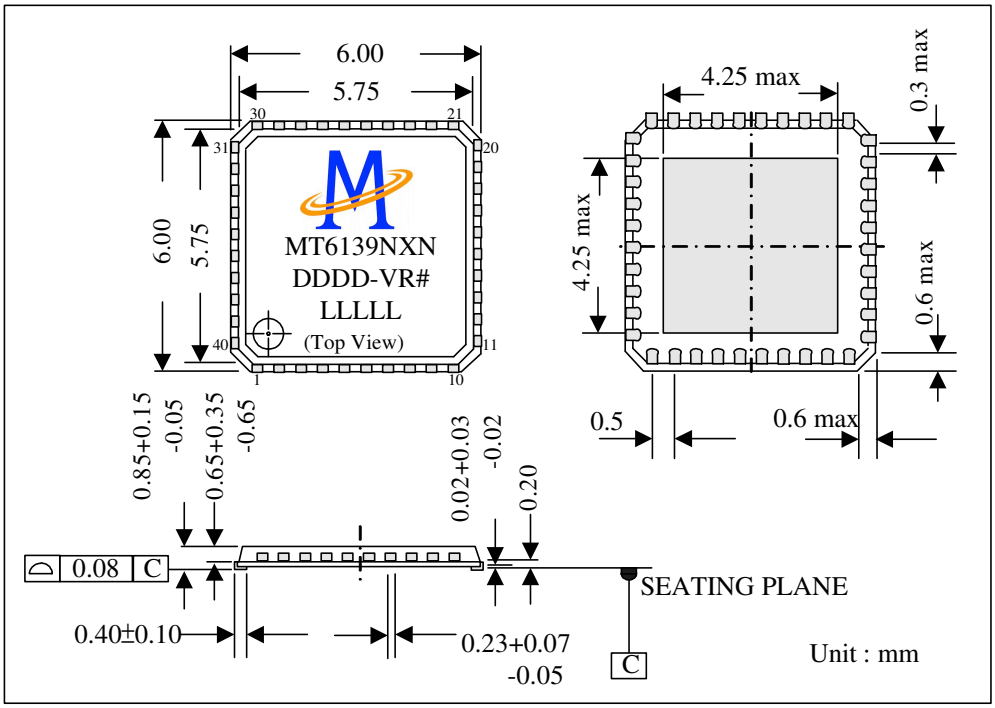
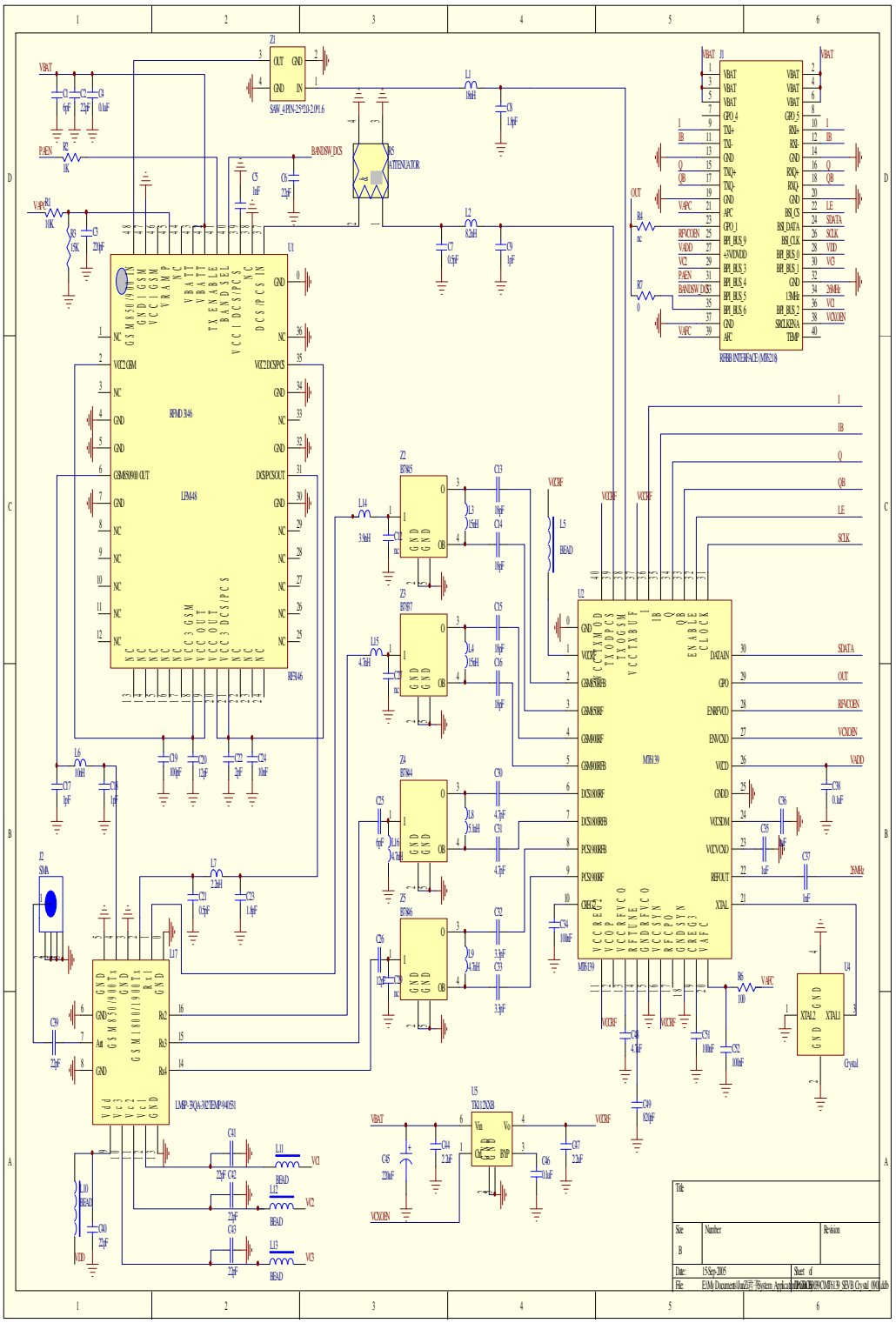


Figure 2 Package dimension

12 Application Circuit



Bibliography references

1. MT6139 3-wire setting programming guide.