Confidential B

MEDIATEK

MT6235 Design Notice V2-3

2008/07

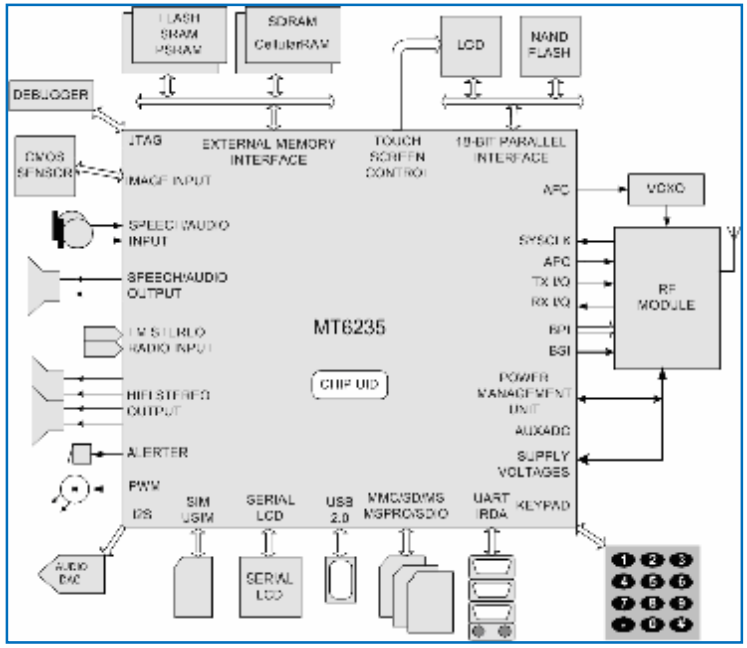
Outline

- MT6235 Main Features & Package
- Design Notice
- Tool/SW version that supports MT6235 development
- Snapshot of MT6235 Reference Phone
- Layout Notice
- Appendix : MT6235 Chip Features
- Appendix : Common Audio Design notice
- Appendix : MT6235Memory Support Plan
- Appendix : MT6235/6238/6239 LCM Design Guide

MT6235 Main Feature

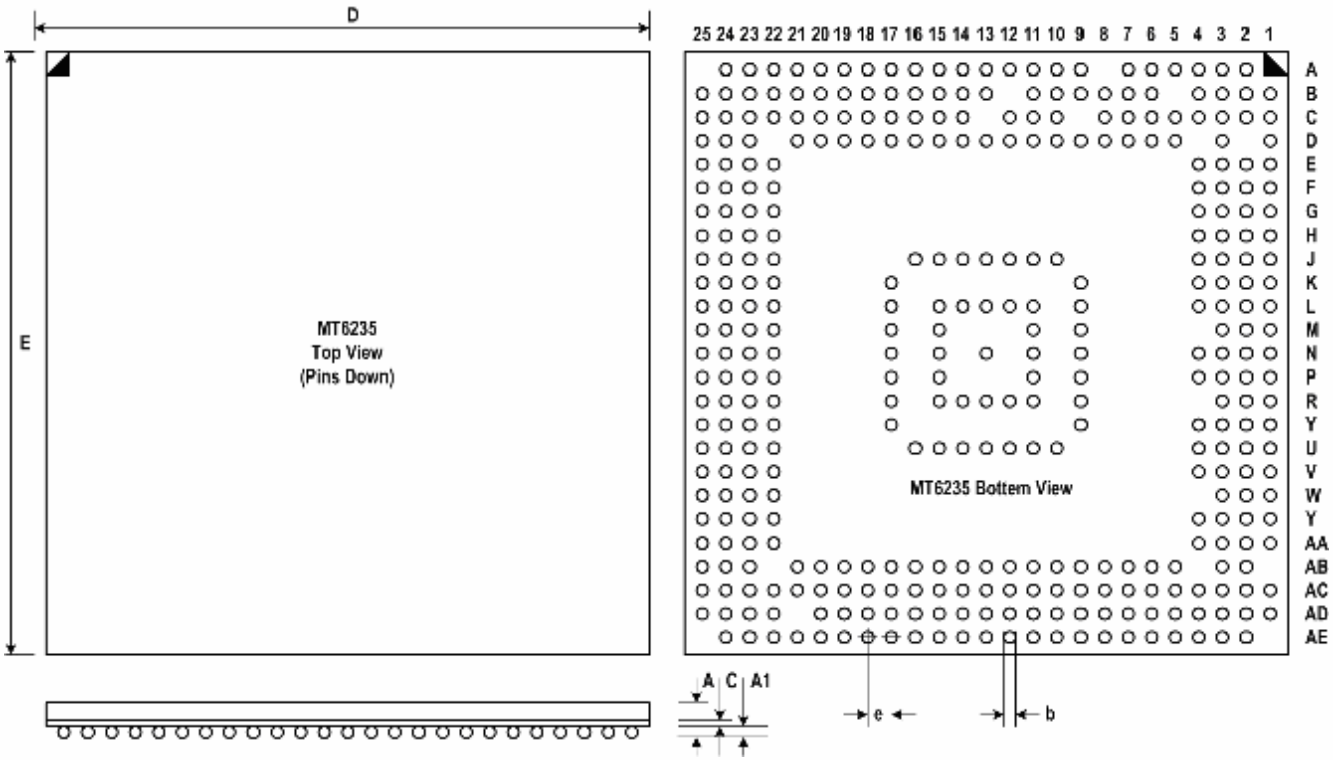
- EDGE Class12, GPRS Class 12
- ARM926EJ-S 208MHz with cache
- PMU / Touch panel driver integrated
- 2M / 1.3M / VGA camera (YUV)
- Chip UID – 315 bit
- FR, EFR, HR, AMR speech codec
- Support up to 16.77M color WQVGA LCM
- Excellent melody format support
  - MIDI, WB AMR, AAC, AAC+, eAAC, digital music
- Polyphonic melody, 64-tone wave table, stereo loudspeaker
- SBC encoder capability supports BlueTooth A2DP function
- Advanced DSP acoustic functionality
  - AEC, noise reduction
- SD/MMC/MS/MSprocard & SDIO support
- USIM support
- Built in USB2.0 (High speed/Device), IrDA
- QWERTY keypad support

- Multi-memory system with more flexibility for phone design
  - NOR/pSRAMwith or without AD MUX; burst mode of up to 104 MHz supported
  - NAND-boot supported
  - NAND data storage supported
  - LPSDRAM supported



Typical application of MT6235

MT6235 Package



Body Size		Ball Count	Ball Pitch	Ball Dia.	Package Thk.	Stand Off	Substrate Thk.
D	E	N	e	b	A (Max.)	A1(Nom.)	C
13	13	362	0.5	0.3	1.2	0.21	0.36

Design Notice – PMU LDO (1/4)

Power	Available Vout (V)	Max current (mA)	Output capacitor (F)
VCORE	1.2/0.9 (DC/DC)	350	4.7u
VM	1.8/2.8	300	4.7u
VCAM_A	1.5/1.8/2.5/2.8	250	4.7u
VCAM_D	1.3/1.5/1.8/2.8	75	1u
VRF	2.8	350	4.7u
VA	2.8	125	4.7u
VTCXO	2.8	40	1u
VIO	2.8	100	1u
VBT	2.8/3.0	100	1u
VUSB	3.3	75	1u
VSIM	1.8/3.0	80	1u
VRTC	1.2	0.02	100n

VCORE, VA, VIO should dedicated for BB power supply due to they built-in internal voltage-sense feedback function.

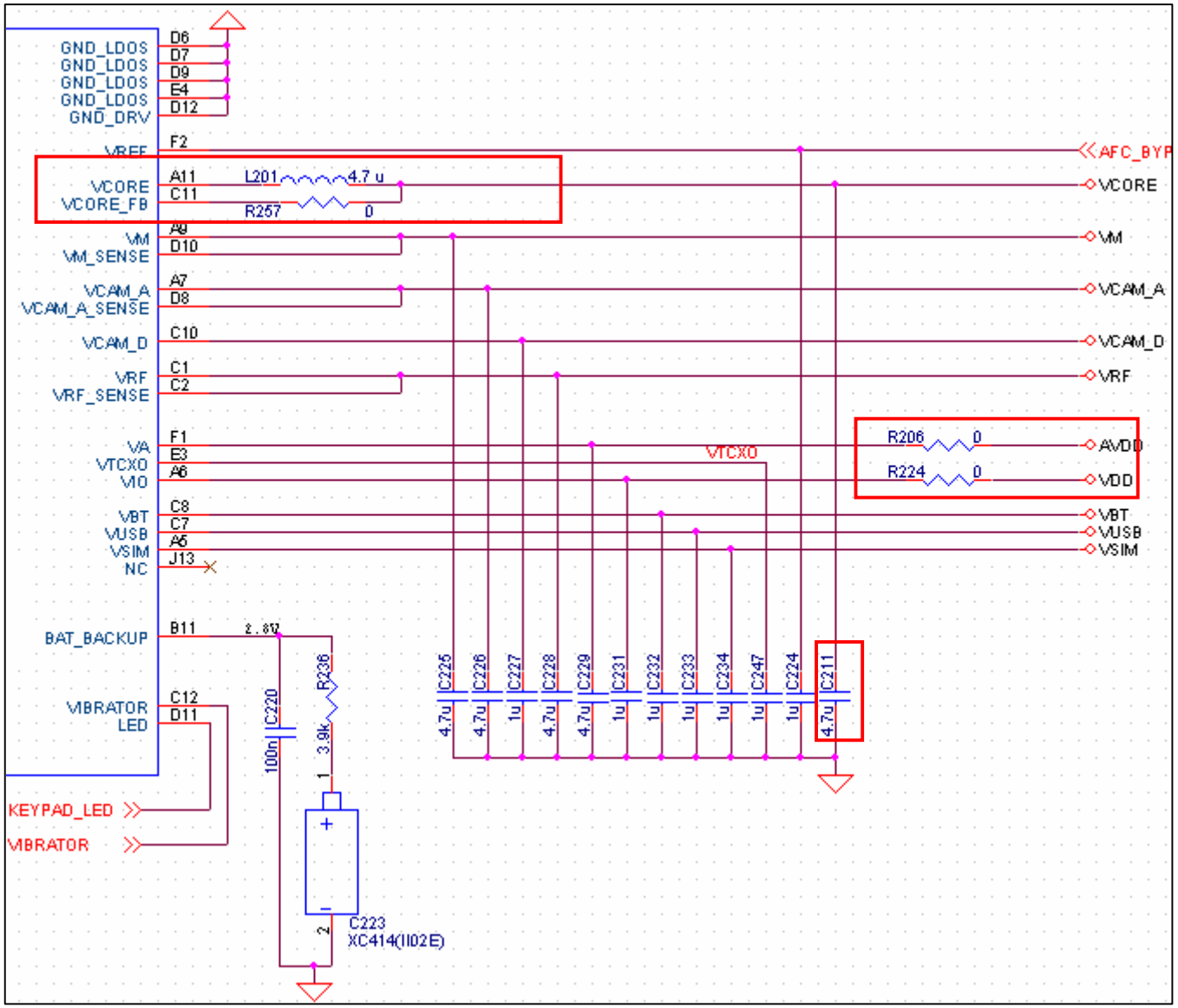
Notice: VA, VIO can be used only for low current consumption application (Ex: FM, NAND, LCM, and pull-high voltage)

Please don't connect VA/VIO to external IC power supply with high current consumption.

Design Notice – PMU LDO (2/4)

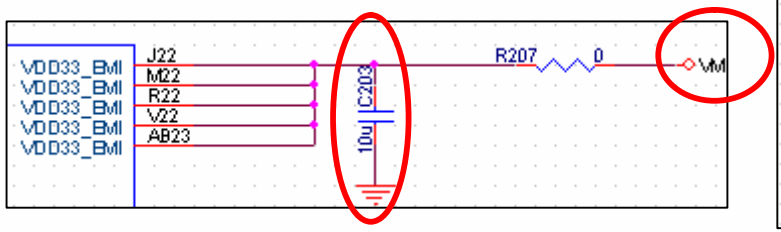
As for VCORE, please keep L201, R257 and C211 closer to BB.

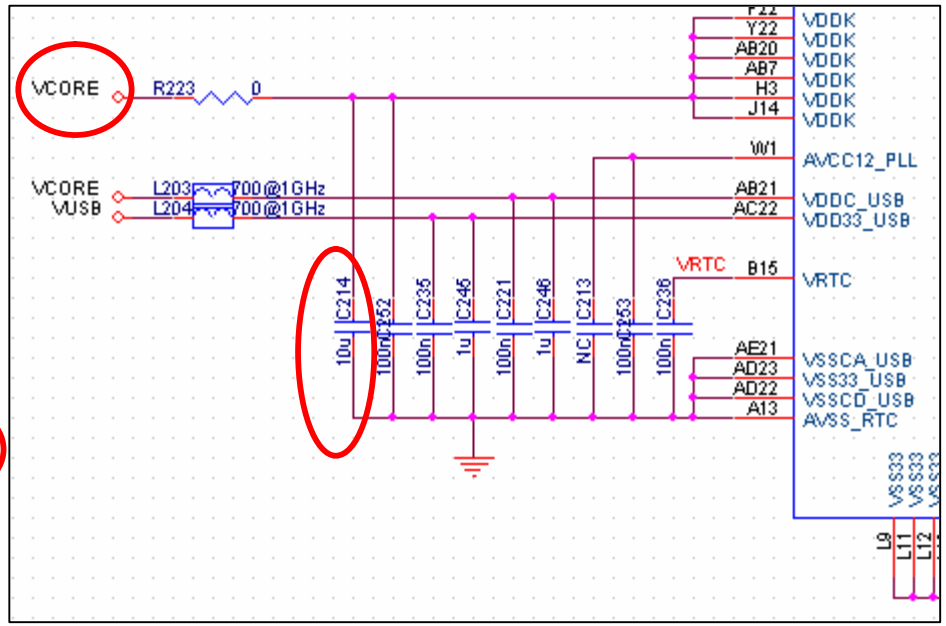
Please also reserve 0ohm in AVDD and VDD trace to debug low power issue.



Design Notice – PMU LDO (3/4)

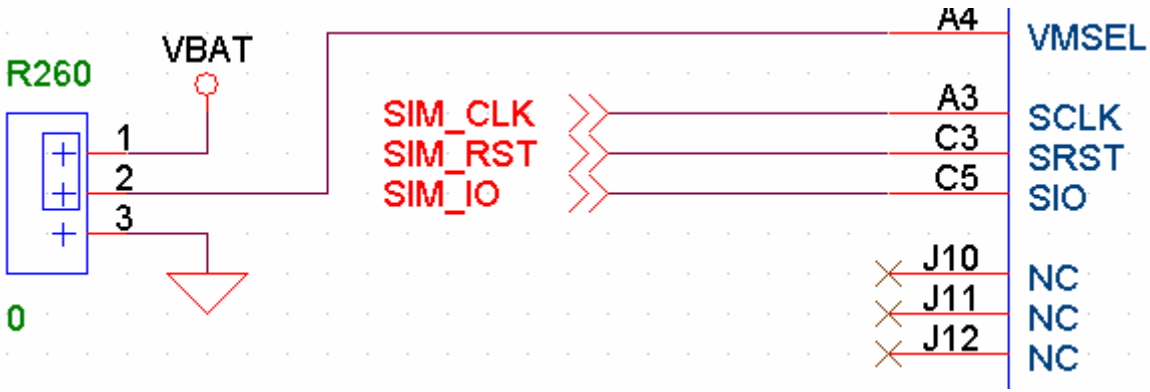
For stable external memory access, please add 10uF(0603) bypass cap in Vmand Vcoreof BB input side.





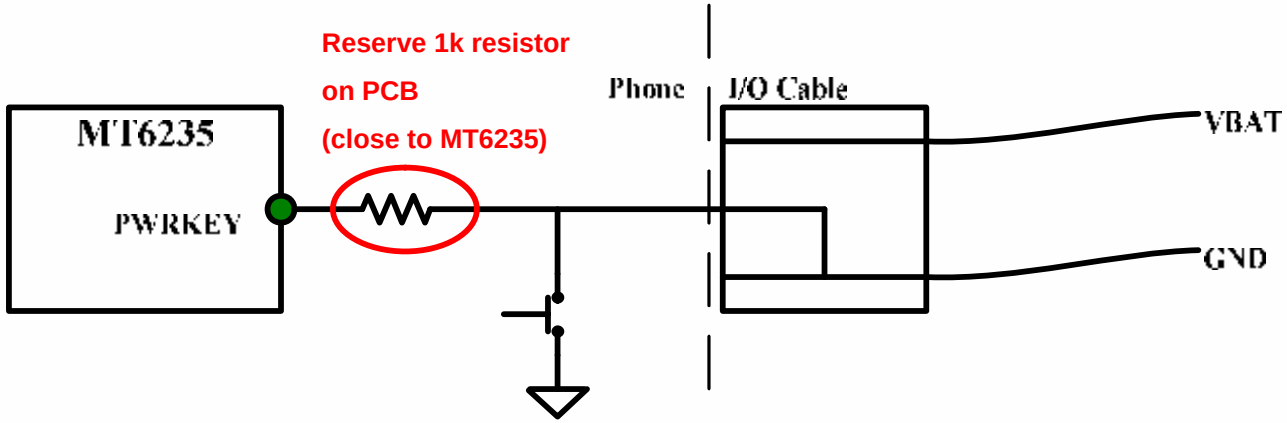
Notice: You can delete several “reserved 0 Ω” in power related circuit.
Please refer to:
ENTRY LEVEL EDGE MUSIC PHONE_20080701_ORCAD10.DSN

Design Notice – PMU LDO (4/4)



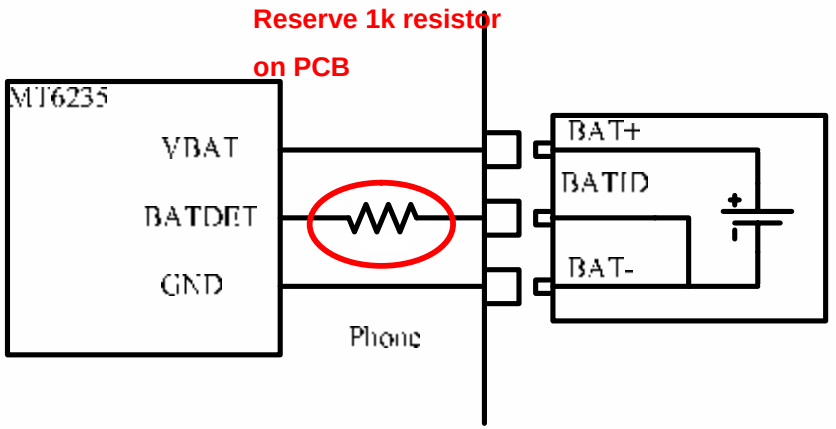
For VMSEL selection,
H(VBAT) for 2.8V memory device
L(GND) for 1.8V memory device

Design Notice – Power (1/2)

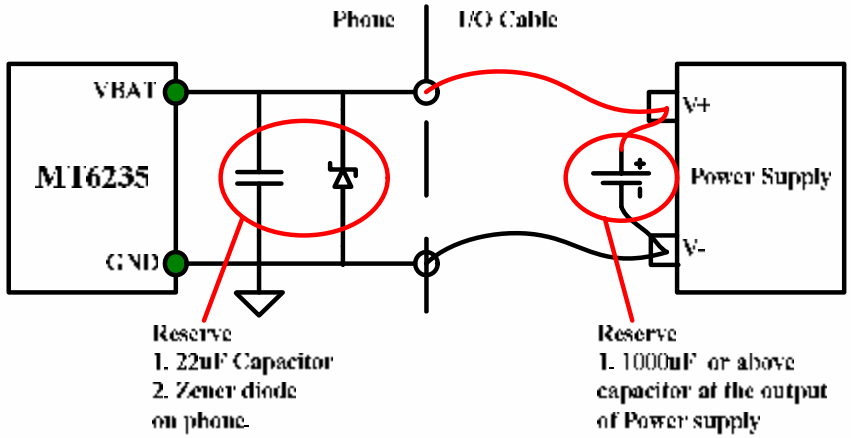


Please reserve 1k resistor on phone PCB to protect **PWRKEY** no matter if PWRKEY connect to any I/O connector or not.

Please reserve 1k resistor on phone PCB to protect **BATDET** pin if BATDET is used to detect battery.



Design Notice – Power (2/2)



MT6235 has lower VBAT voltage rating. (Max. 4.3V.) Some protection should reserve to prevent the damage by voltage surge.

•Design notice in Phone side:
1. Add 22uF capacitor.
2. Add Zenerdiode (5.6V) to protect the IC against low frequency voltage surge. Put it between battery connector and MT6235.
Notice: Using 5.6V zenerwill introduce some leakage when VBAT = 4.2V.
ex. 5.6V zenerCZRU52C5V6, will have extra 5uA leakage.

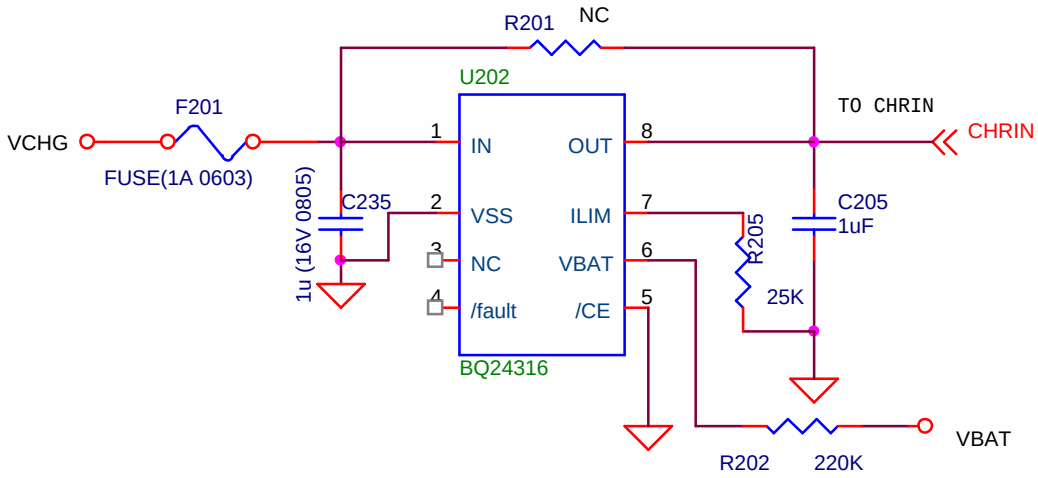
•Design notice in Power Supply side:
Add 1000uF (or above) capacitor at the output of the power supply to reduce the voltage bounce caused by long power cable.

Design Notice – Charger Protection

	MT6305B	MT6318	MT6235	External OVP/OCP
Max. Charger Input	15V	15V	9V	30V
Charger OVP Point	9V	9V	7V	6.8V

MT6235 same as MT6223 at OVP point and Max charger input.

External OVP/OCP:



Notice :

You can get better charger protection by using external OVP/OCP device.

Design Notice – External Memory Interface

MT6235	External Memory (NOR+PSRAM)	External Memory (SDRAM)	Remark
EA[0:26]	EA[0:26]	A[0:12]	NO NEED to shift
EA14 EA15	---	BA0 BA1	CANNOT use EA13
ED[0:15]	ED[0:15]	D[0:15]	
EADMUX	* see remark	* see remark	L for non-ADMUX H for ADMUX
ECS[0:3]_B	NOR_CS# PSRAM_CS#	CS#	
ERD_B	NOR_OE# PSRAM_OE#	---	
EWR_B	NOR_WE# PSRAM_WE#	WE#	
ED_CLK ED_CLK_B	---	CLK CLK#	
EC_CLK	NOR_CLK	---	
ECKE	---	CKE	
EADV_B	NOR_ADV#	---	
ECAS_B	---	CAS#	
ERAS_B	---	RAS#	
EDQM0	PSRAM_LB#	LDQM	
EDQM1	PSRAM_UB#	UDQM	
EDQS0	---	---	
EDQS1	---	---	
EWAIT	NOR_WAIT	---	

EA0 of MT6235 is word address, no need to shift when connect 16 bit memory device.

MT6235 can support ADMUX or non-ADMUX memory device.

MT6235 can support NOR-booting or NAND-booting.

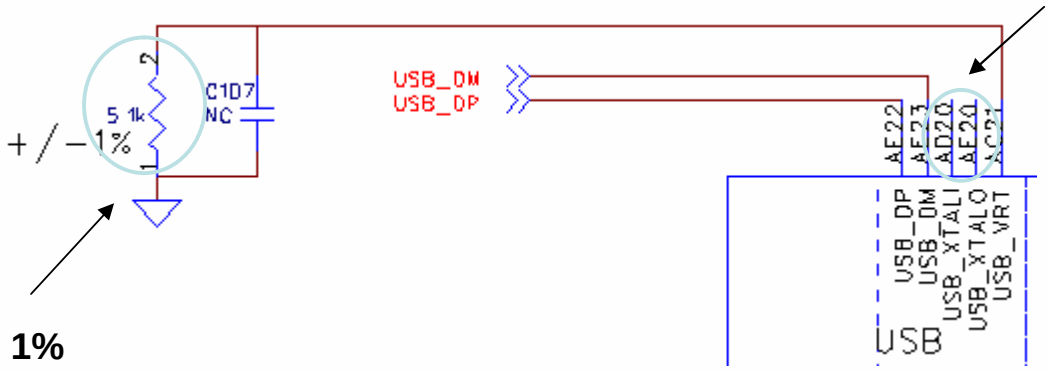
MT6235 Still not support DDR

DDR memoryhave been supported from MT6238.

Design Notice – USB2.0 Device (1/2)

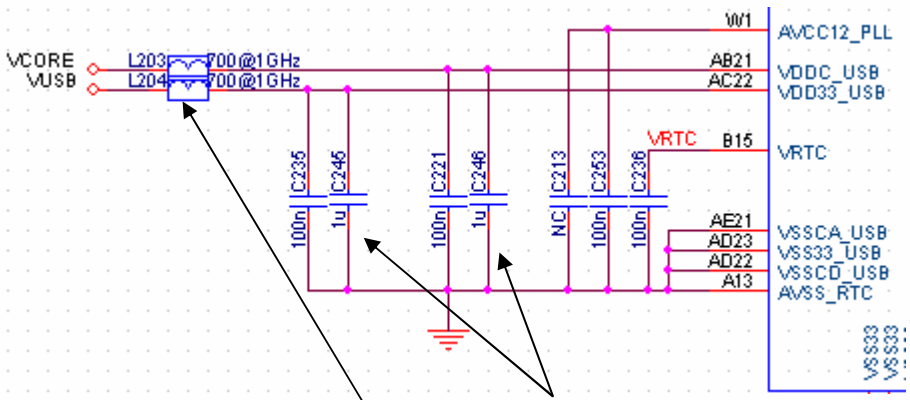
(Due to USB2.0 SCH/Layout are both critical, please refer to "MTK_USB_Application_Notes" to get more information)

Reserved for external crystal



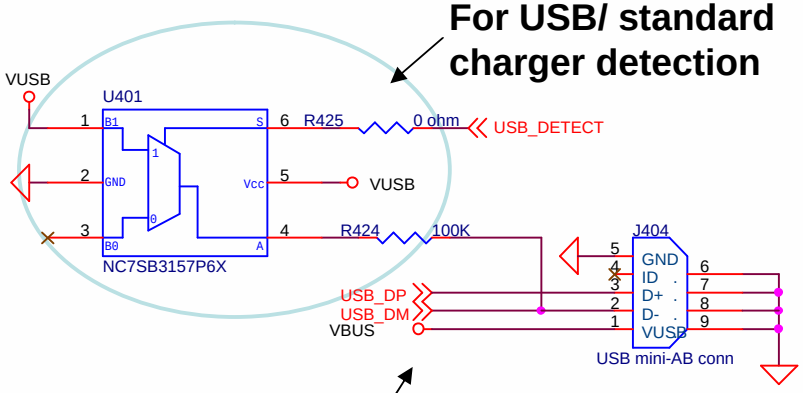
Must be 5.1K ohm, 1%
Place close to IC

MT6235 support USB2.0 but without OTG, please pay more attention to the difference of USB block between MT6235 and MT6238.



Reserve bead and bypass capacitor for USB 1.2, 3.3V Power

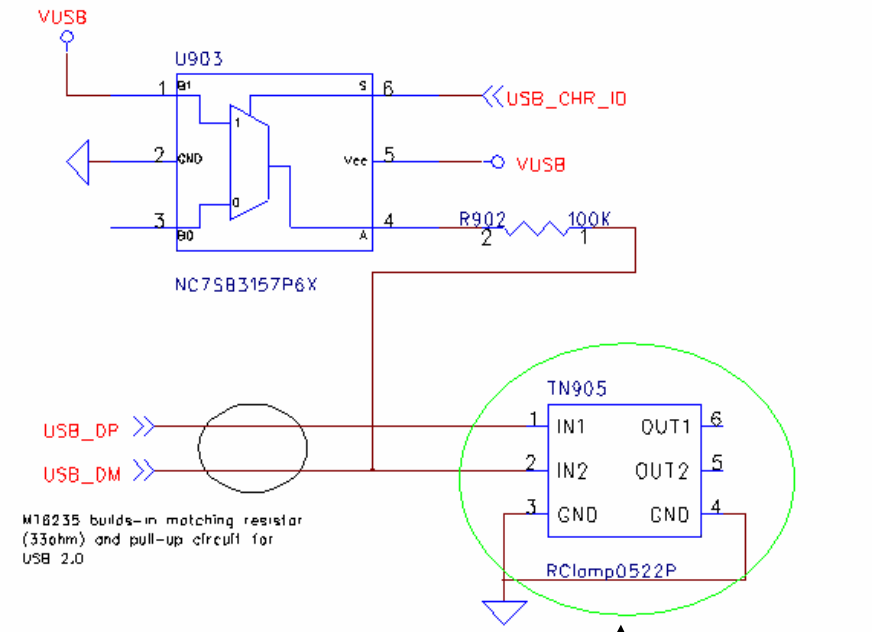
For USB/ standard charger detection



No need of ID + EINT pins

Design Notice – USB2.0 Device (2/2)

(Due to USB2.0 SCH/Layout are both critical, please refer to "MTK_USB_Application_Notes" to get more information)



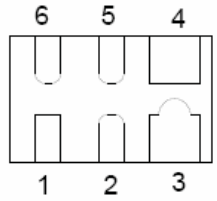
RClamp0522P: ESD protect component for High speed signal trace.

SemtechUltra Low Capacitance TVS Arrays

Low capacitance: **0.3pF** typical (I/O to I/O)

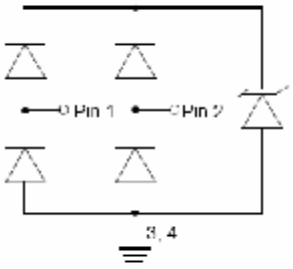
Pin Identification and Configuration

RClamp0522P



Pin	Identification
1 - 2	Input Lines
5 - 6	Output Lines (No Internal Connection)
3 - 4	Ground

Circuit Diagram - RClamp0522P

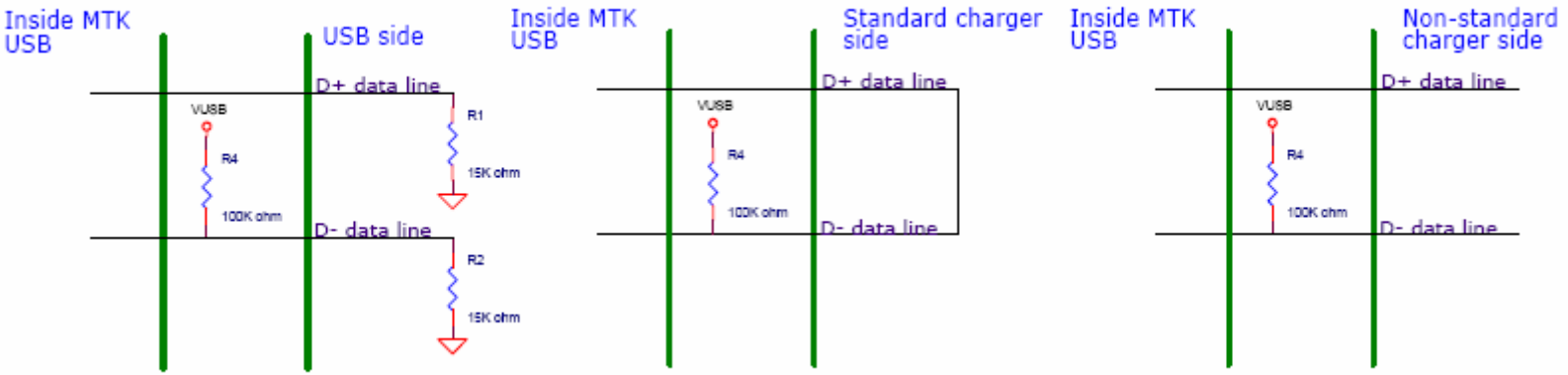


2-Line Protection

Design Notice – USB/ Charger Detection(1/2)

1. To check whether it is USB charger or ACcharger

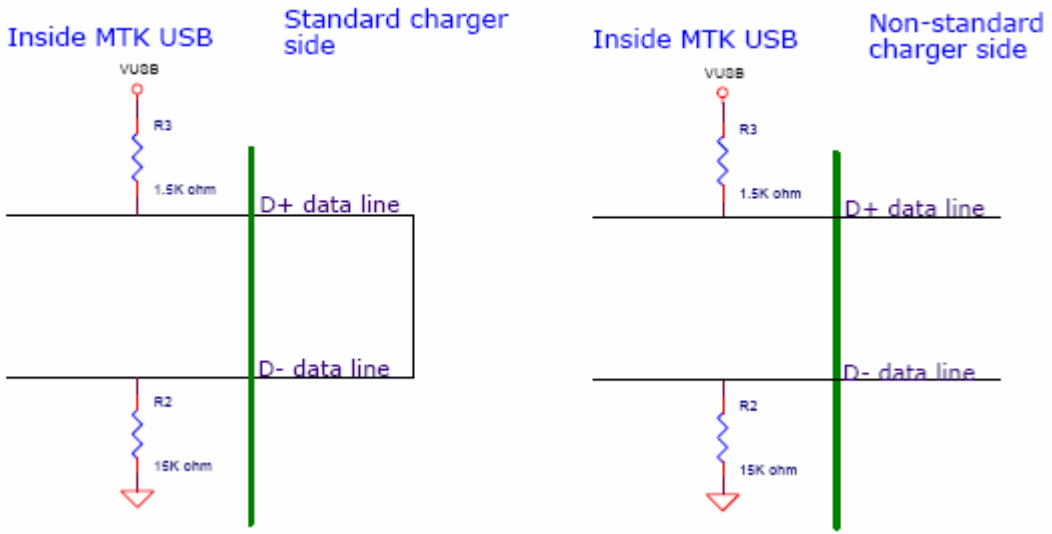
- When charger interrupt happens, turn on external Analog switch, enable D- external 100K ohm pull high resistor
- And check the polarity of D-, if the D-is LOW, it is USB charger, otherwise it is a standard or a non-standard charger



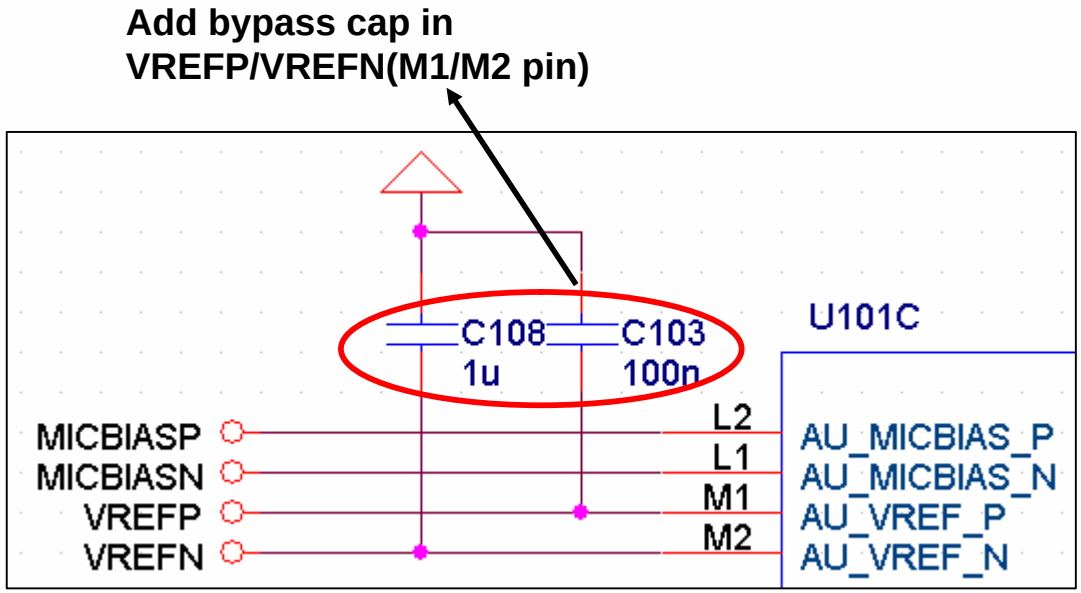
Design Notice – USB/ Charger Detection(2/2)

2. Then check whether it is standard or non-standard charger

- Turnon D+internal1.5K ohmpull high resistorandD-internal 15K ohm pull low resistor at the same time
- Check D-polarity, If the D-is HIGH, it is a standard charger, otherwise itis a non-standard charger



Design Notice – Audio



- VREF_N is used for 1/2Vdd reference decoupling capacitor (1uF), this is used to enhance audio DAC+bufferPSRR and audio performance.

- Vref_Pis used for Voice reference decoupling capacitorf(100nF) for generating MICBIAS, and also is voice ADC/DAC reference.

Design Notice – ADC

ADC channel	Function	Pin out
AUXADC_0	External ADC channel	T4
AUXADC_1	External ADC channel	U2
AUXADC_2	External ADC channel	U4
AUXADC_3	External ADC channel	V2
AUXADC_4	ISENSE (Fix)	x (internal)
AUXADC_5	BATSENSE (Fix)	x (internal)
AUXADC_6	CHRIN (Fix)	x (internal)

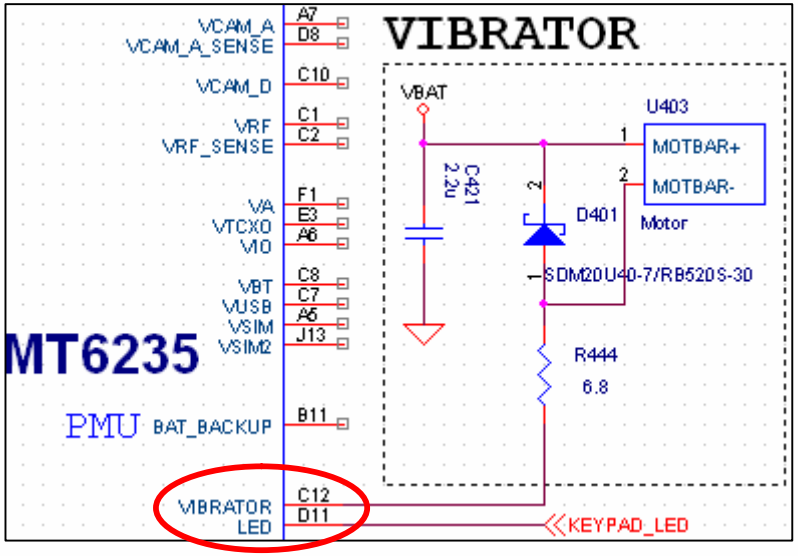
MT6235 has one more External ADC pin than MT6223, And the internal fix channel for Isense/Batsense/Vchrin also different between MT6235 and MT6223.

PS: ADC4 for Vchrin, ADC5 for Isense, and ADC6 for Batsensein MT6223.

Design Notice – PWM

Pin name (External pin)	PWM channel (Internal)	Power domain	Pin out
LED	PWM1		D11
VIBRATOR	PWM2		C12
PWM0	PWM3	VDD33	AC10
PWM1	PWM4	VDD33	AB10
PWM2	PWM5	VDD3_CAM	AC5
PWM3	PWM6	VDD3_CAM	AE5

The power domain of external PWM2 and PWM3 are VDD33_CAM, so PWM2 and PWM3 must be dedicated for camera usage.

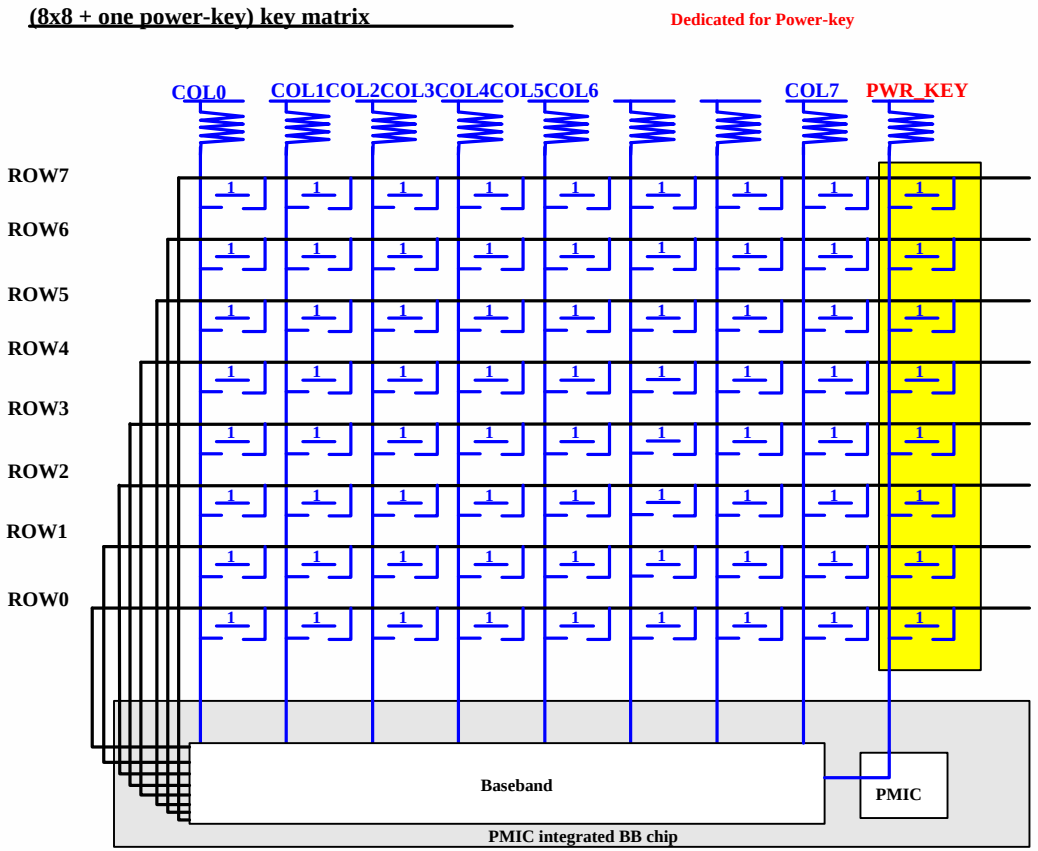


Driver	Current Capability
LED	150 mA
VIBRATOR	250 mA

"LED" and "VIBRATOR" are Open Drain N-MOS with dedicated internal PWM channel for dimming control.

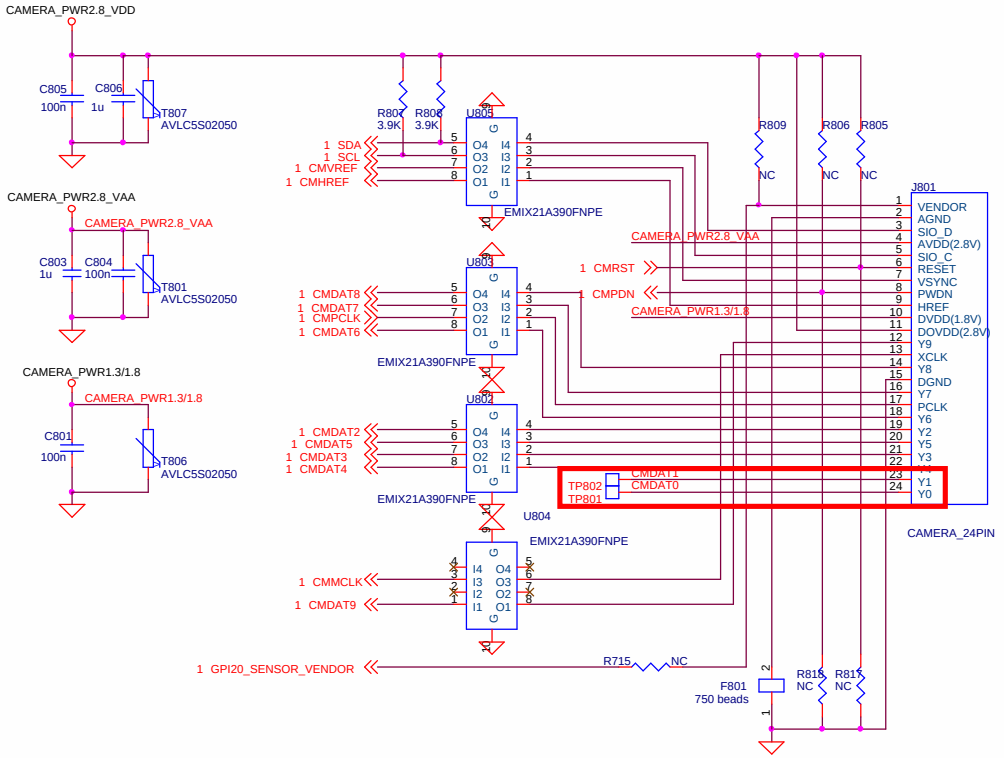
Design Notice – QWERTY Keypad

- MT6235 is 8x8 matrix, except COL8
- **COL8** is dedicated for POWER_KEY (internal connection)
- So, the matrix can support up to 8x8+1=65 keys, which is called QWERTY keypad

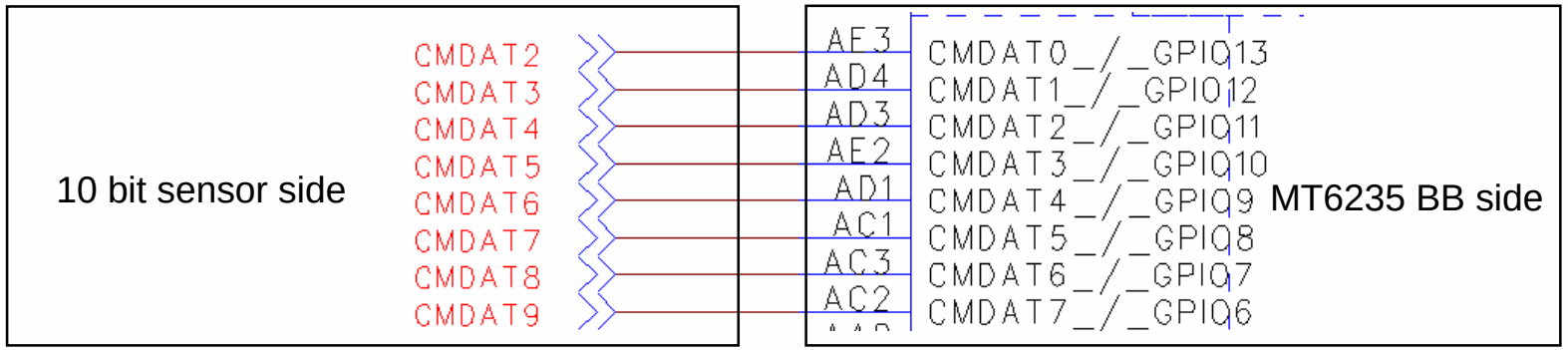


Design Notice – Camera Interface

- Up to 2M pixels
- 8bit YUV interface supported
- Suggest to reserveEMI filter on Camera/LCM bus

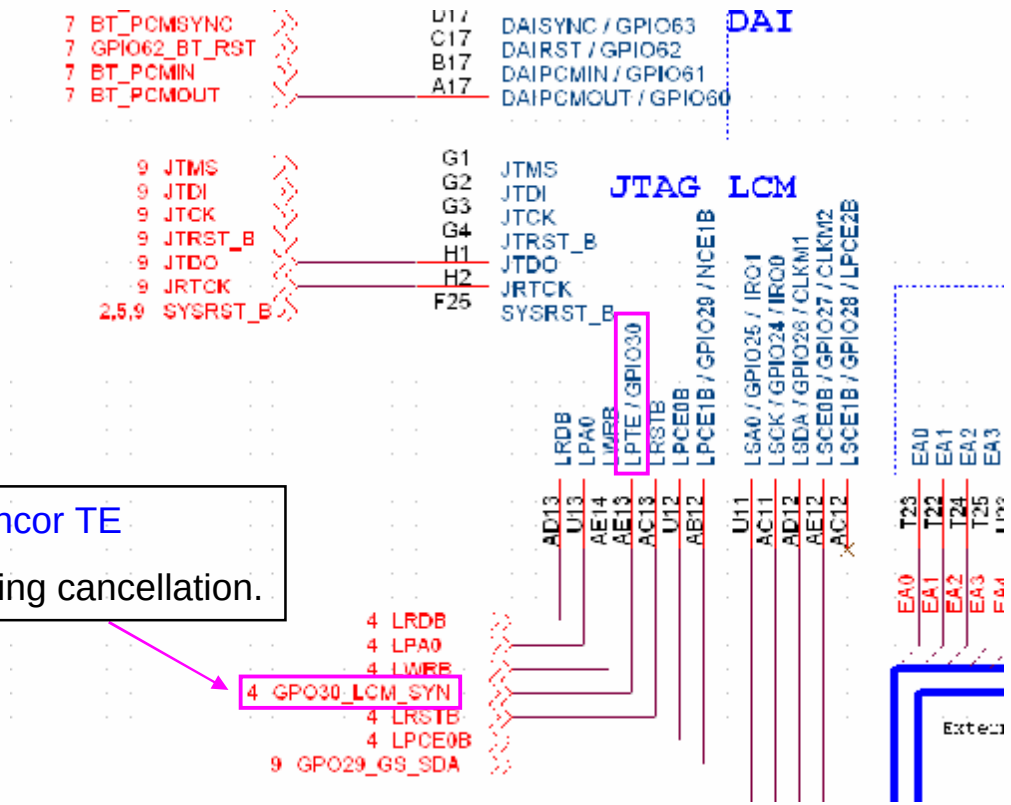


Be careful of the mapping of MSB/LSB between MT6235 8 bit camera I/F and 10 bit sensor.



Design Notice – LCM dedicated pin LPTE

For HW design



Connect LCM F_syncor TE

to BB LPTE for tearing cancellation.

For SW setting (make file)

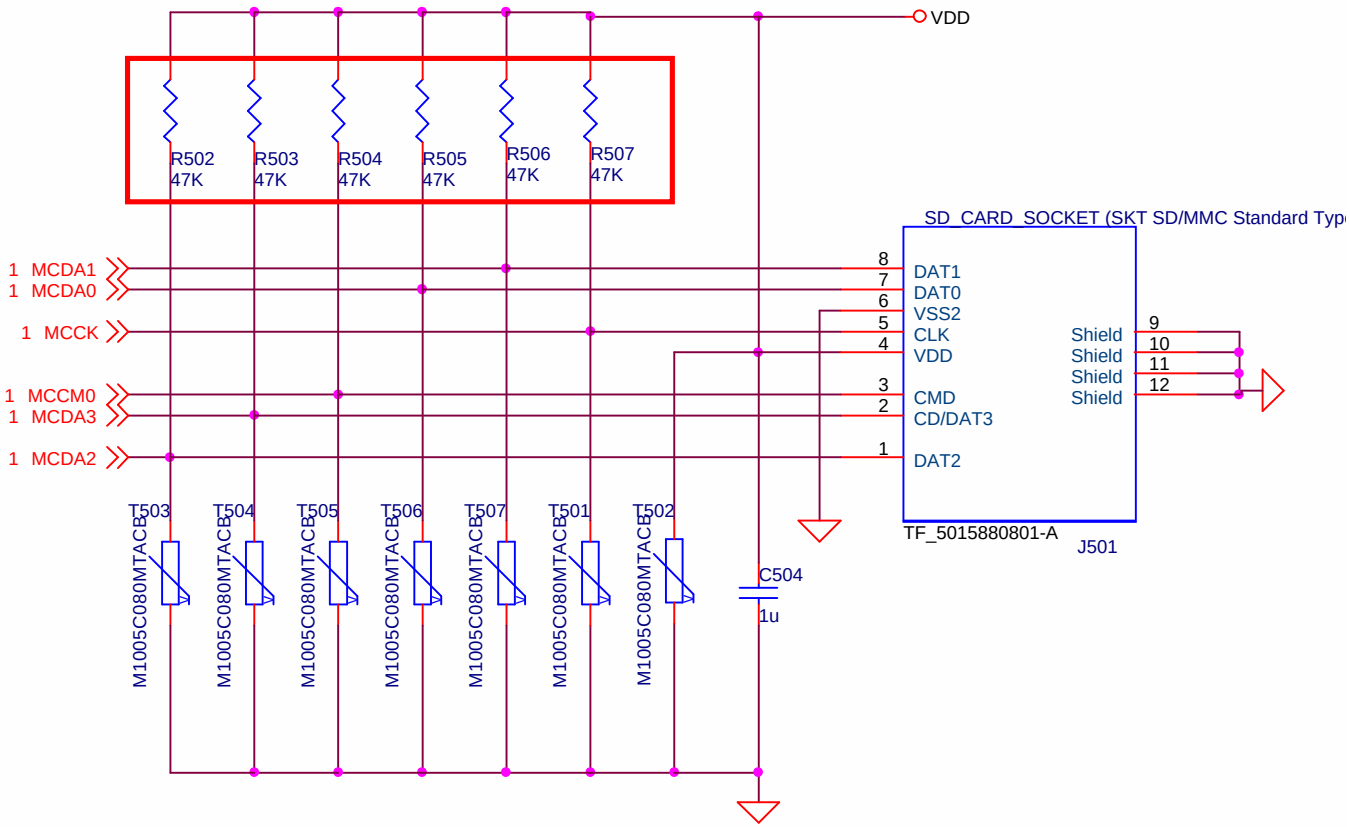
SYNC_LCM_SUPPORT = TRUE **# TRUE or FALSE**

 # TRUE if Sync mode LCM is applied and FALSE if Sync mode LCM isapplied.

Notice : Both HW and SW need to be checked!!

Design Notice – Memory Card Interface

•For better interoperability and stability, please reserve 47k ohm in each memory card interface line.

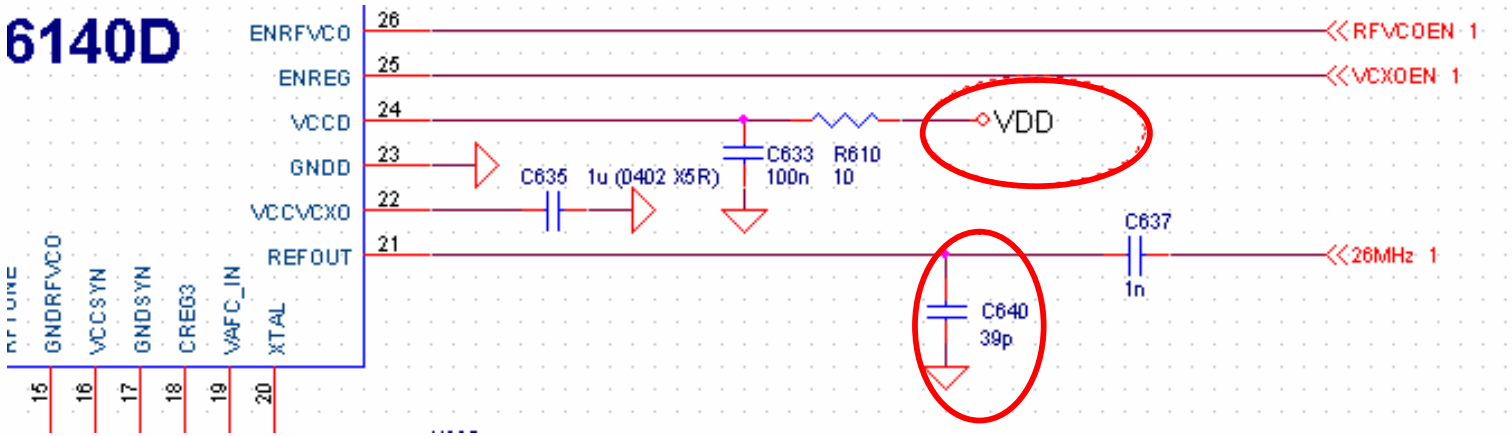


Design Notice – H/W Configuration Pins

Pin name	Pin out	Normal mode	TEST mode	Enable Security	Burn EFUSE
TESTMODE	B14	L	VDD	L	L
XBOOT	AE7	L	L	L	L
SECU_EN	AD6	L	L	VDD	L
FSOURCE	AA1	L	L	L	VBAT
VCCQ	Y4	VDD	VDD	VDD	VBAT

- For normal usage, please configure above pins to be “Normal mode”.
- TESTMODE, XBOOT, FSOURCE, VCCQ are only for debugging, please follow above configuration.
- You can enable MT6235 security function by setting SECU_EN=VDD

Design Notice – RF

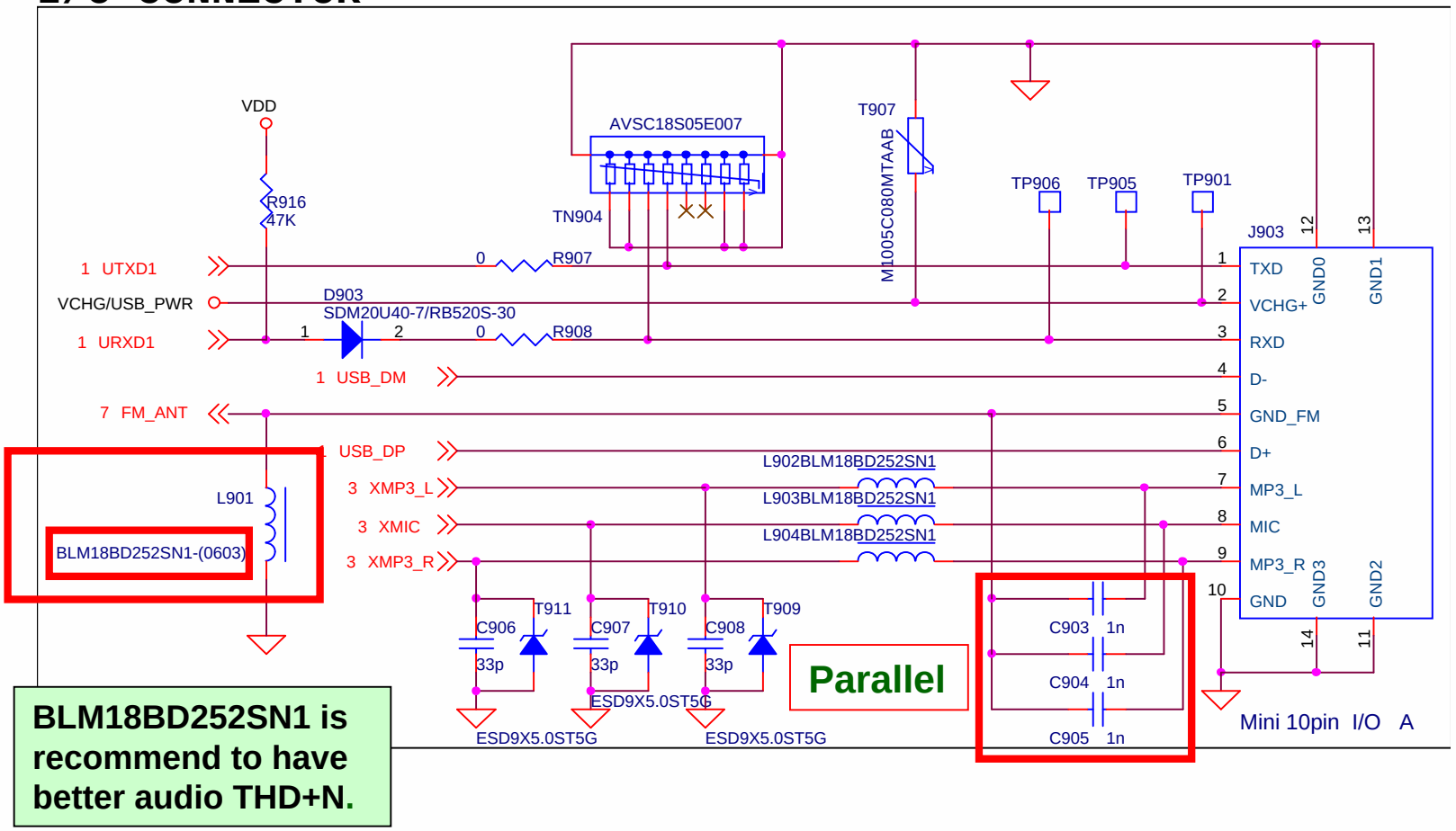


To avoid customer's confusion, pin24 named VCCD of MT6140 has been changed from AVDD to VDD in our latest Reference Design.

Moreover，C640 also changed from defaultNC to 39p.

Design Notice – I/O (1/2)

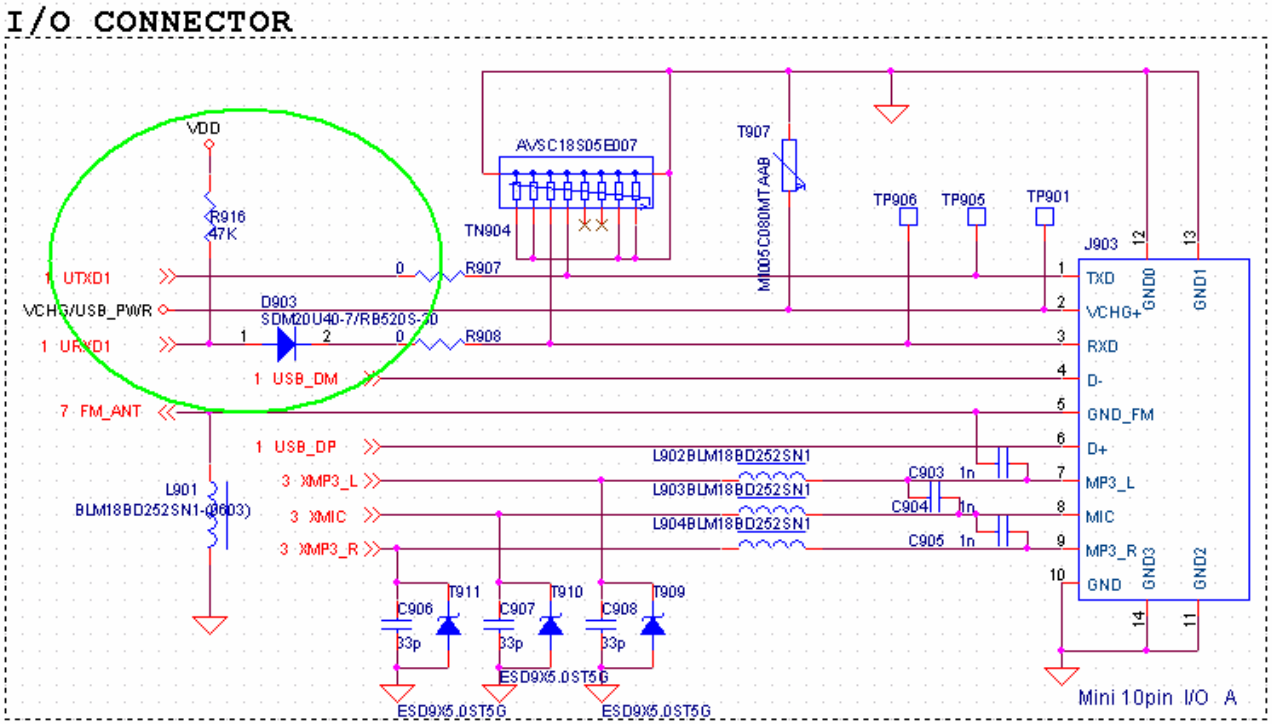
I/O CONNECTOR



BLM18BD252SN1 is recommend to have better audio THD+N.

FM and Crosstalk performance should trade-off, Audio I/O circuit is recommend as above, if FM function design-in.

Design Notice – I/O (2/2)



Q : What is the purpose of “Diode and PullHighresistor ”?

A : When plug-in download, there is the leakage patch from PC to Basebandthrough the UART_RX of download cable.

Then the leakage will cause all GPIO’sabnormal voltage through VDD power domain.

But this issue will only happen during someone plug-in download cable. So you don ’t need to reserve above circuit if you have no any concern about this issue.

Design Notice – GPIO selection (1/7)

1. Pull-Up / Pull-Down selection :

- Choose GPIO with suitable PU/PD after reset state for application
  - Ex : As for enable pin of audio amplifier, please choose GPIO with PD after reset state

2. Power domain of IO supply selection :

- Choose GPIO with suitable power domain of IO supply for application
  - GPIO0 ~ GPIO18 : VDD33_CAM
  - GPIO24~ GPIO38 : VDD33_LCD
  - GPIO64~GPIO66 : VDD33_EMI
  - GPIO67~GPIO75 : VDD33_MC
  - Other GPIOs : VDD33

3. Please choose suitable GPIO for peripheral IC :

- Please choose GPIOswith matched direction, pull-up/pull-down, data inversion, data output, gpiomode after reset state for peripheral IC application

Design Notice – GPIO selection (2/7)

Be careful of following GPIO'spower domain of IO supply :

Following GPIOswill be workable during VDD33_CAM is active

Ball Map	NAME	PU/PD	Power Domain	Aux Func.0	Aux Func.1	Aux Func.2	Aux Func.3
AA2	CMRST	PU/PD	VDD33_CAM	GPIO0	O:CMRST	O:CLKM0	O:DSP_GPO0
AA3	CMPDN	PU/PD	VDD33_CAM	GPIO1	O:CMPDN		O:DSP_GPO1
AB3	CMVREF	PU/PD	VDD33_CAM	GPIO2	I:CMVREF		
AB2	CMHREF	PU/PD	VDD33_CAM	GPIO3	I:CMHREF		
AA4	CMPCLK	PU/PD	VDD33_CAM	GPIO4	I:CMPCLK		
AB6	CMMCLK	PU/PD	VDD33_CAM	GPIO5	O:CMMCLK		
AC2	CMDAT7	PU/PD	VDD33_CAM	GPIO6	I:CMDAT7		
AC3	CMDAT6	PU/PD	VDD33_CAM	GPIO7	I:CMDAT6		
AC1	CMDAT5	PU/PD	VDD33_CAM	GPIO8	I:CMDAT5		
AD1	CMDAT4	PU/PD	VDD33_CAM	GPIO9	I:CMDAT4		
AE2	CMDAT3	PU/PD	VDD33_CAM	GPIO10	I:CMDAT3		
AD3	CMDAT2	PU/PD	VDD33_CAM	GPIO11	I:CMDAT2		
AD4	CMDAT1	PU/PD	VDD33_CAM	GPIO12	I:CMDAT1		
AE3	CMDAT0	PU/PD	VDD33_CAM	GPIO13	I:CMDAT0		
AC4	CMFLASH	PU/PD	VDD33_CAM	GPIO14	O:CMFLASH		
AE4	SCL	PU/PD	VDD33_CAM	GPIO15	SCL		
AD5	SDA	PU/PD	VDD33_CAM	GPIO16	SDA		
AC5	PWM2	PU/PD	VDD33_CAM	GPIO17	O:PWM2		
AE5	PWM3	PU/PD	VDD33_CAM	GPIO18	O:PWM3		

Design Notice – GPIO selection (3/7)

Be careful of following GPIO'spower domain of IO supply :

Following GPIOswill be workable during VDD33_LCD is active

Ball Map	NAME	PU/PD	Power Domain	Aux Func.0	Aux Func.1	Aux Func.2	Aux Func.3
AC11	LSCK	PU/PD	VDD33_LCD	GPIO24	O:LSCK	O:DSP_GPO2	I1: IRQ0
U11	LSA0	PU/PD	VDD33_LCD	GPIO25	O:LSA0	O:DSP_GPO3	I1: IRQ1
AD12	LSDA	PU/PD	VDD33_LCD	GPIO26	O: LSDA	O:CLKM1	
AE12	LSCE0B	PU/PD	VDD33_LCD	GPIO27	O:LSCE0B	O:CLKM2	
AC12	LSCE1B	PU/PD	VDD33_LCD	GPIO28	O:LSCE1B	O:LPCE2B	
AB12	LPCE1B	PU/PD	VDD33_LCD	GPIO29	O:LPCE1B	O:NCE1B	
AE13	LPTE	PU/PD	VDD33_LCD	GPIO30	I:LPTE		
AD14	NLD17	PU/PD	VDD33_LCD	GPIO31	NLD17		
AC14	NLD16	PU/PD	VDD33_LCD	GPIO32	NLD16		
AC18	NRNB	PU/PD	VDD33_LCD	GPIO33	I1:NRNB		
AB18	NCLE	PU/PD	VDD33_LCD	GPIO34	O:NCLE		
AE19	NALE	PU/PD	VDD33_LCD	GPIO35	O:NALE		
AD19	NWEB	PU/PD	VDD33_LCD	GPIO36	O:NWEB		
AC19	NREB	PU/PD	VDD33_LCD	GPIO37	O:NREB		
AB19	NCEB	PU/PD	VDD33_LCD	GPIO38	O:NCE0B		

Design Notice – GPIO selection (4/7)

Be careful of following GPIO'spower domain of IO supply :

CLKM5, CLKM6, CLKM7 will be workable during VDD33_EMI is active

GPIO67~GPIO75 will be workable during VDD33_MC is active

Ball Map	NAME	PU/PD	Power Domain	Aux Func.0	Aux Func.1	Aux Func.2	Aux Func.3
AD25	EA26	PU/PD	VDD33_EMI	GPIO64	EA26	O:CLKM5	
T17	EADMUX	PU/PD	VDD33_EMI	GPIO65	I:EADMUX	O:CLKM6	
K17	MFIQ	PU/PD	VDD33_EMI	GPIO66	I1:nFIQ	O:CLKM7	
B16	MCCM0	PU/PD	VDD33_MC	GPIO67	MC0CM0		
C16	MCDA0	PU/PD	VDD33_MC	GPIO68	MC0DA0		
D16	MCDA1	PU/PD	VDD33_MC	GPIO69	MC0DA1		
J16	MCDA2	PU/PD	VDD33_MC	GPIO70	MC0DA2		
C15	MCDA3	PU/PD	VDD33_MC	GPIO71	MC0DA3		
D15	MCCK	PU/PD	VDD33_MC	GPIO72	MC0CK		
J15	MCPWRON	PU/PD	VDD33_MC	GPIO73	O:MC0PWRON	O:CLKM8	
C14	MCWP	PU/PD	VDD33_MC	GPIO74	I1:MC0WP	O:CLKM9	
D14	MCINS	PU/PD	VDD33_MC	GPIO75	I:MC0INS		

Design Notice – GPIO selection (5/7)

Be careful of the GPIO default PU/PD value after reset state

(Valid when GPIO is input mode)

GPIOnGPIO pull up/down selection
0 GPIOspull down is selected
1 GPIOspull up is selected

GPIO +0400h	GPIO pull-up/pull-down select register 1															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO15	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	GPIO8	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GPIO +0440h	GPIO pull-up/pull-down select register 2															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO31	GPIO30	GPIO29	GPIO28	GPIO27	GPIO26	GPIO25	GPIO24	GPIO23	GPIO22	GPIO21	PGIO20	GPIO19	GPIO18	GPIO17	GPIO16
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	1

GPIO+0480h	GPIO pull-up/pull-down select register 3															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO47	GPIO46	GPIO45	GPIO44	GPIO43	GPIO42	GPIO41	GPIO40	GPIO39	GPIO38	GPIO37	GPIO36	GPIO35	GPIO34	GPIO33	GPIO32
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	0

GPIO+04C0h	GPIO pull-up/pull-down select register 4															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO63	GPIO62	GPIO61	GPIO60	GPIO59	GPIO58	GPIO57	GPIO56	GPIO55	GPIO54	GPIO53	GPIO52	GPIO51	GPIO50	GPIO49	GPIO48
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	0	0	0	0	0	1	1	1	1	1	1	0	1	1

GPIO+0500h	GPIO pull-up/pull-down select register 5															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					GPIO75	GPIO74	GPIO73	GPIO72	GPIO71	GPIO70	GPIO69	GPIO68	GPIO67	GPIO66	GPIO65	GPIO64
Type					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset					1	1	1	1	1	1	1	1	1	1	0	0

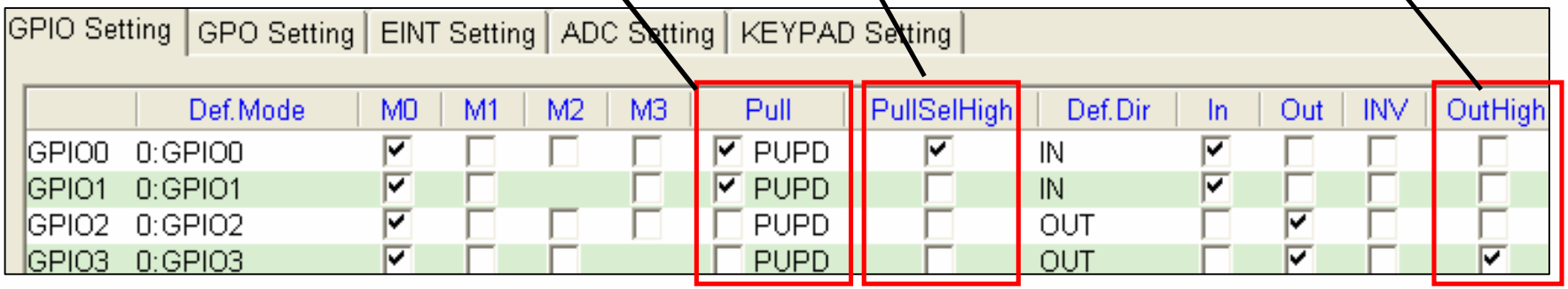
Design Notice – GPIO selection (6/7)

Notice of Drv_Toolusage

After Enable/Disable PU/PD, you can change the PU/PD value by changing "PullSetHigh".
(Only valid when GPIO is input mode)

"Pull" can enable/disable PU/PD, then GPIO will be the default PU/PD value after reset state.
(Only valid when GPIO is input mode)

"OutHigh" can change the default output level.
(Only valid when GPIO is output mode)



In above example :
GPIO0 will be PU in input mode
GPIO1 will be PD in input mode (GPIO1 = PD default)
GPIO2 will be Low in output mode
GPIO3 will be High in output mode

Design Notice – GPIO selection (7/7)

Design Phase (common rule)

Schematic:

1. Adopt internal DC-DC.
2. Set the appropriate **GPIO** settings.
   For example: I2C, PU for active high functions; PD for active low functions, PD for LDO enable.
3. Add a 0Ω resistor into the VDD, and AVDD power traces.

Driver:

1. Set unused **GPIO** pins to **GPI** mode (in Drv_Tool)
2. Set to **GPI** mode if the function is deactivated (for each driver).
3. Disable **GPIO** PU/PD.

Load builds:

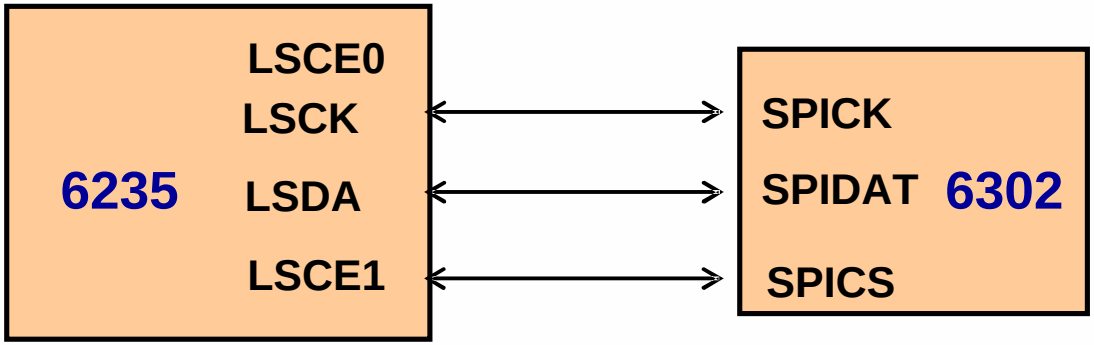
1. Builds load (After 06A.W0648) and onward support DCM and software enhancements.
2. Builds load (After 07A.W0724) support 1R7PM.

Debug Phase

Design Notice – Dual SIM application

(1) MT6235 + MT6302

- MT6235 controls MT6302 via SPI I/F
- To use GPIOssimulating SPI is practicable.



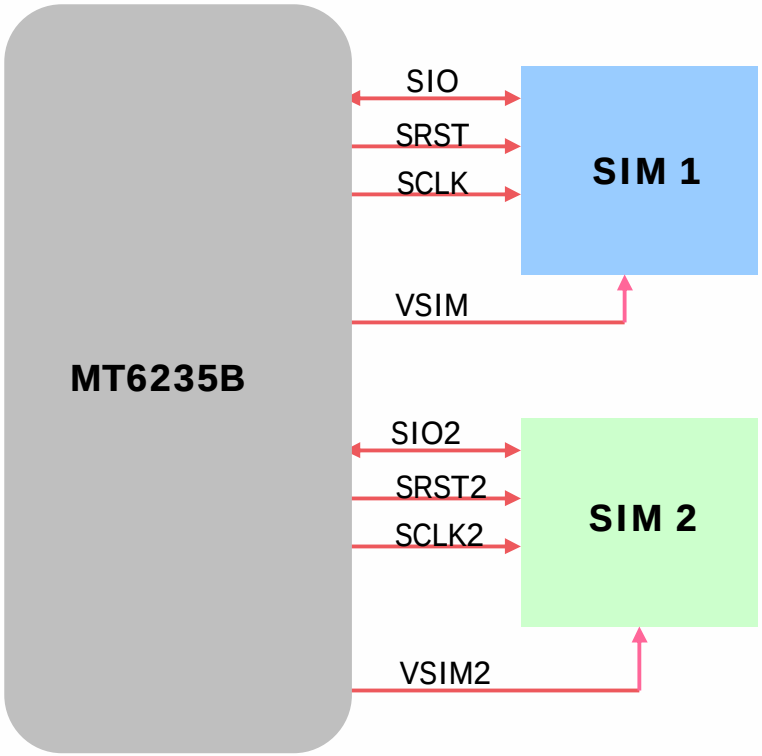
	MT6226/26M/27	MT6225	MT6228/29	MT6235
LSCE1	GPIO20	GPIO33	GPIO24	GPIO28
LSCK	GPIO16	GPIO29	GPIO20	GPIO24
LSDA	GPIO18	GPIO31	GPIO22	GPIO26

- Please refer to “MT6302 (Dual SIM) Introduction” to get more information
- MT6235+MT6302 doesn't pass MTK'sinternal SQC

Design Notice – Dual SIM application

(2) MT6235B

- MT6235B add 4 more pins to support dual SIM application



	Pin	Name	MT6235	MT6235B
SIM1	A5	VSIM	support	support
	A3	SCLK	support	support
	C3	SRST	support	support
	C4	SIO	support	support
SIM2	J13	VSIM2	NC	support
	J10	SCLK2	NC	support
	J11	SRST2	NC	support
	J12	SIO2	NC	support

Notice : Please contact WCP/SM to get detailed MT6235B schedule

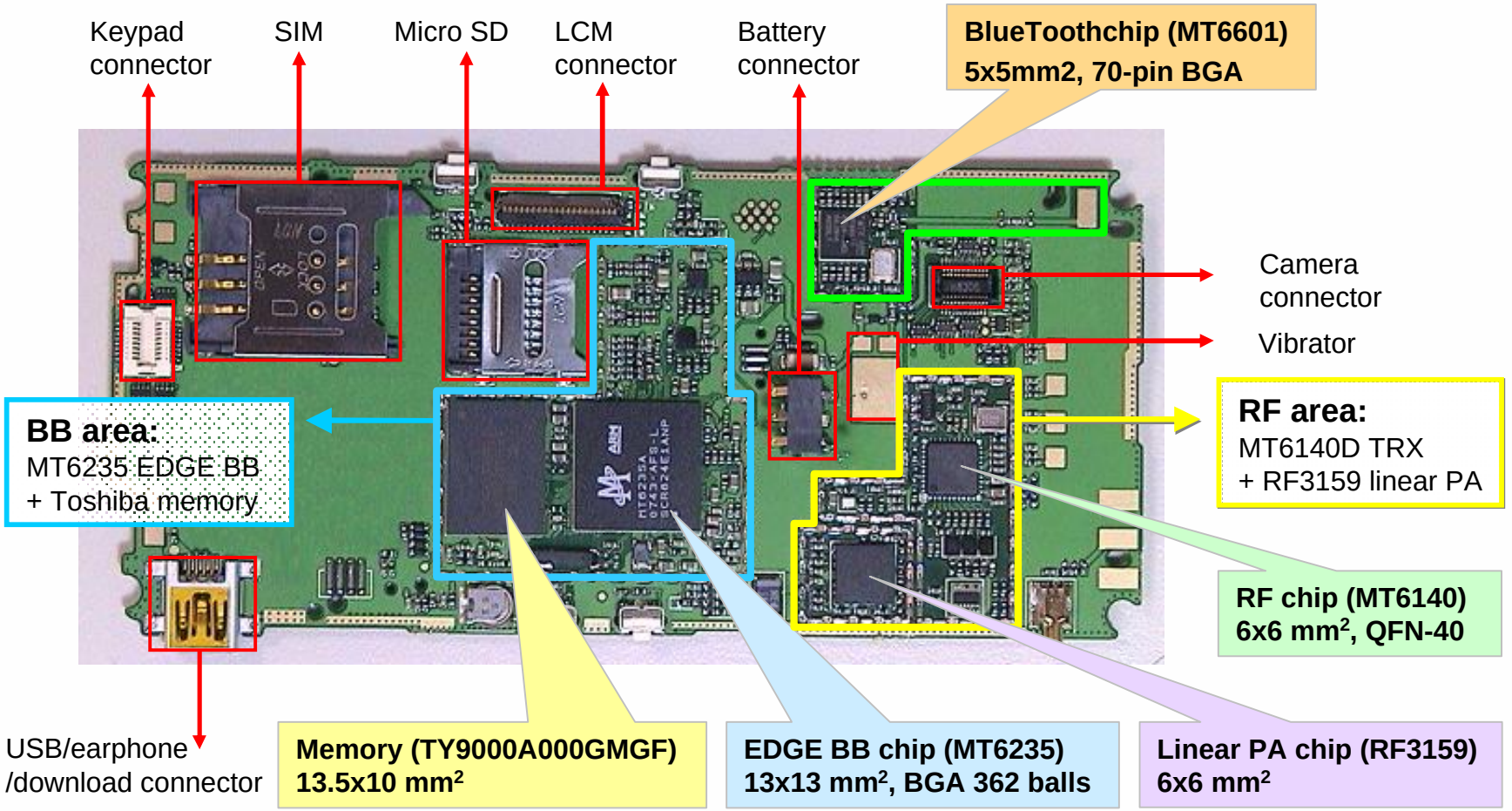
Tool version that supports MT6235 development

Tool	Support version
ATE Tool (including SN WRT Tool)	After **0748**
META Tool (including META_DLL)	After **5.0748.0**
META_APP_DLL Tool	After **5.0748.0**
MultiportDownloadTool	After **5.0748.0**
FlashTool	After **FlashTool_v3.0808.00**

SW version that supports MT6235 development

Function	Support version
MT6235 with NAND booting	**08A0824MP**
MT6235 with NOR booting	**08A0828MP**
MT6235 + MT3326 + A-GPS	**08A0832MP**
MT6235 + MT6302	**08AW0828 -> Only workable version** **08AW0832 ->MP version**
MT6235 + MT3326 + A-GPS + MT6302	**08AW0836MP**

Snapshot of MT6235 Reference Phone



Layout Notice (1/5)

0. PCB layer : MT6235 support 6 layer PCB layout.

1. Power trace :

(1) VRTC , VSIM , VTCXO : 10mil at least

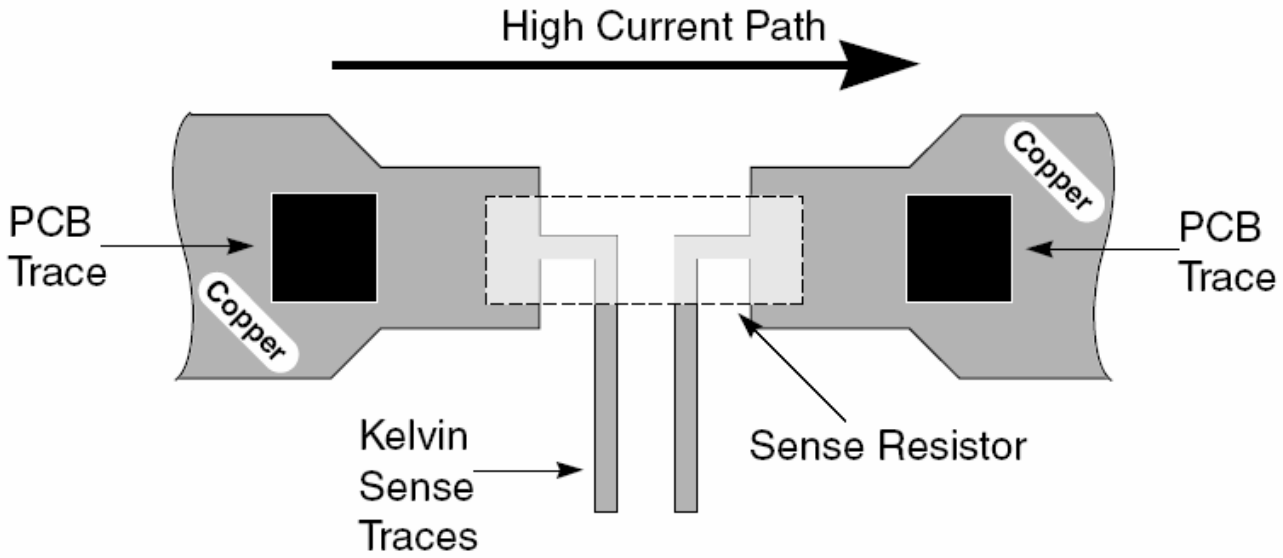
(2) VCORE : 25mil at least

(3) VDD , AVDD , VMEM : 20mil at least

(4) Charging path : VCHG~VBAT: 40mil at least

(5) Connect Rsenseto BATSENSE(B3 pin) directly [Please refer to following diagram]

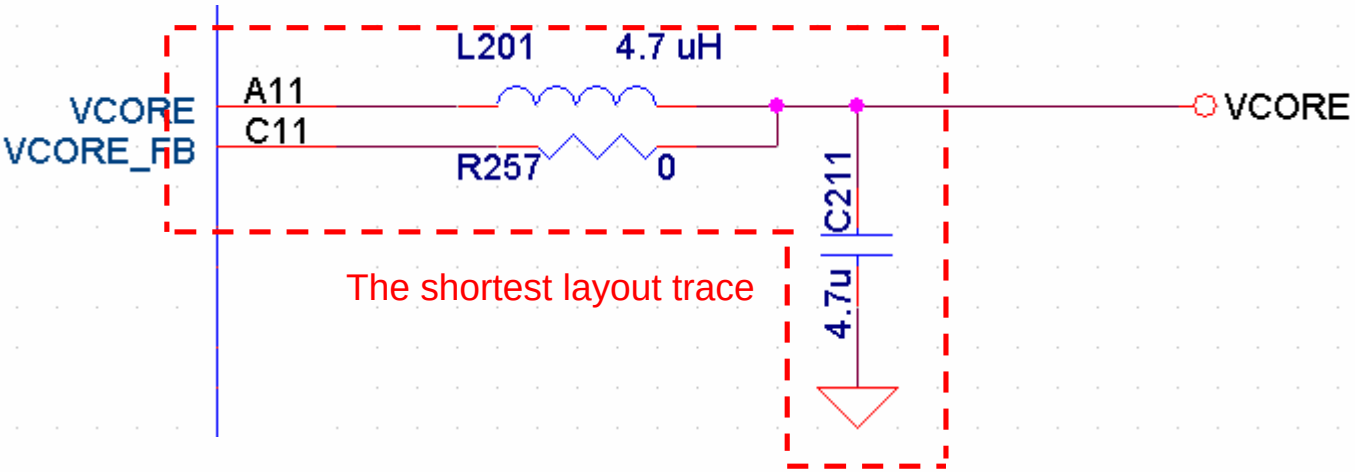
Connect Rsenseto ISENSE(D5 pin) directly [Please refer to following diagram]



Layout Notice (2/5)

1. Power trace :

(6) Due to VCORE built-in internal DC/DC, please layout the shortest layout tracefrom BB output to inductance to bypass capacitor.



Layout Notice (3/5)

2. Audio trace : (Common rule [1]Protect following traces by GND on upper layer, lower layer, left side, and right side [2]Avoid the crossover with power traces)

(1) SPKP0/SPKN0 , MICP0/MICN0 , MICP1/MICN1 : Differential line ; the same trace length

(2) MP3_OUTR/MP3_OUTL : The same trace length

(3) AU_FMINR/AU_FMINL : The same trace length ; Use GND to separate AU_FMINR and AU_FMINL

(4) MICBIASP/MICBIASN

3. RF related trace : (Common rule [1]Protect following traces by GND on upper layer,lower layer, left side, and right side [2]Avoid the crossover with power traces)

(1) IP/IQ, QP/QN : Differential line ; the same trace length

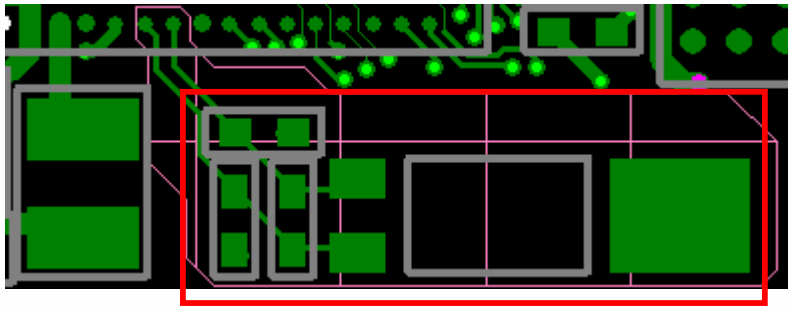
(2) APC, AFC

(3) SYSCLK(26MHz)

Layout Notice (4/5)

4. Clock related trace: (Common rule [1]Protect following traces by GND on upper layer, lower layer, left side, and right side [2]Avoid the crossover with power traces)

(1) 32kHz :The shortest path ;Please keep the layer clearance in upper and lower layer relatedto 32kHz traces ;Keep Xout and Xin trace away from Vcoredue to Vcore built-in internal DC/DC. (Notice: they are close in the IC ball map:Xin-A14,Xout-A15,Vcore-A11)



(2) EC_CLK , ED_CLK, ED_CLKB

(3) CMMCLK, CMPCLK, DAICLK, SIMCLK : No need to protect those traces by GND, but please keep 8mil distance with other traces

Layout Notice (5/5)

5. USB related trace : Due to USB2.0 SCH/Layout are both critical, please refer to "MTK_USB_Application_Notes" to get more information

6. Reset related trace : (Common rule [1]Please keep 8mil distance with other traces [2]Please keep 50mil distance withshielding case and PCB edge.

(1) RESETB , SYSRST_B

(2) WATCHDOG

(3) LRSTB

(4) SIMRST

Issue Case Study

Issue Case Study - 1

[Issue description]

Customer use PWM2 to be the LCM backlight, but PWM2 cannot work normally after power on

[Rootcause]

The PWM2 power domain of IO supply is VDD33_CAM. It means that PWM2 cannot work during VDD33_CAM is inactive. Normally VDD33_CAM will be turned on after user enter camera mode.

[Solution]

Change the LCM backlight from PWM2 to PWM0 or PWM1

Ball Map	NAME	PU/PD	Power Domain	Aux Func.0	Aux Func.1	Aux Func.2	Aux Func.3
AC10	PWM0	PU/PD	VDD33	GPIO39	O:PWM0		AC10
AB10	PWM1	PU/PD	VDD33	GPIO40	O:PWM1	I:BSI_RFIN	AB10
AC5	PWM2	PU/PD	VDD33_CAM	GPIO17	O:PWM2		
AE5	PWM3	PU/PD	VDD33_CAM	GPIO18	O:PWM3		

Issue Case Study - 2

[Issue description]

1. Customer choose GPIO44 to be the BT_PWR_EN of MT6611.
2. Press the PowerKeyshortly then release PowerKey, the phone is still no power on.
3. MT6611 will have about 30mA leakage.

[Rootcause]

When user press the PowerKeyshortly, the GPIO44 will become high in a short time. Then GPIO44 will turn on MT6611 internal LDO always. Due to phone not power on normally, so this this LDO will cause about 30mA leakage.

[Solution]

Change the BT_PWR_ENfrom GPIO44(Reset=PU) to GPIO43(Reset=PD)

GPIO+0480h	GPIO pull-up/pull-down select register 3															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO47	GPIO46	GPIO45	GPIO44	GPIO43	GPIO42	GPIO41	GPIO40	GPIO39	GPIO38	GPIO37	GPIO36	GPIO35	GPIO34	GPIO33	GPIO32
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	0

Issue Case Study - 3

[Issue description]

ADC Calibration Fail

[Rootcause]

MT6235 internal use ADC4 for Charger Current Sense, use ADC5 forBattery Voltage Sense, this is similar with MT6223,and different with MT6225 platform.

The Second reason is MT6235 use 0.2Ohmresistor for RSENSE.

[Solution]

Modify Calibration Configure File. The CFG file is located in:

C:\Program Files\MediaTek\Maui META ver xxx\xxx.CFG

Modify the Follow description from:

BATTERY_CHANNEL = 0

CHARGER_CHANNEL = 1

ADC_RESISTANCE = 0.4

To:

BATTERY_CHANNEL = 5

CHARGER_CHANNEL = 4

ADC_RESISTANCE = 0.2

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Appendix :
MT6235 Chip Features

Appendix - MT6235 Chip Function (1/8)

Baseband chip feature list			MT6226	MT6225	MT6228	MT6229	MT6230	MT6235
Modem	GSM	FR	V	V	V	V	V	V
		HR	V	V	V	V	V	V
		EFR	V	V	V	V	V	V
		CSD/F	V	V	V	V	V	V
		CSD/H	V	V	V	V	V	V
	GPRS		Class 12	Class 12	Class 12	Class 12	Class 12	Class 12
	AMR	FR	V	V	V	V	V	V
		HR	V	V	V	V	V	V
	EDGE					Class 12	Class 12	Class 12
	SAIC							V
MCU system	RISC		ARM7EJ-S	ARM7EJ-S	ARM7EJ-S	ARM7EJ-S	ARM7EJ-S	ARM926EJ-S
	Speed		52 MHz	104 MHz	104 MHz	104 MHz	104 MHz	208 MHz
	I-Cache			128Kb	256Kb	256Kb	256Kb	128Kb
	D-Cache				64Kb	64Kb	64Kb	128Kb
	TCM			576Kb	768Kb	768Kb	768Kb	1Mb
	MPU			V	V	V	V	
	MMU							V
	Debug	Software debug	V	V	V	V	V	V
		Coresight						

Appendix - MT6235 Chip Function (2/8)

Baseband chip feature list			MT6226	MT6225	MT6228	MT6229	MT6230	MT6235
DSP	DSP		1	1	1	2	2	2
	Speed		91 MHz	104 MHz	104 MHz	104 MHz	104 MHz	104 MHz
	Speech codec	FR	V	V	V	V	V	V
		HR	V	V	V	V	V	V
		EFR	V	V	V	V	V	V
		AMR FR	V	V	V	V	V	V
		AMR HR	V	V	V	V	V	V
		Wide-band AMR	V	V	V	V	V	V
	CTM		V	V	V	V	V	V
	Noise reduction	UL	V	V	V	V	V	V
		DL		V	V	V	V	V
	Noise suppression		V	V	V	V	V	V
	Echo cancellation		V	V	V	V	V	V
	Echo suppression		V	V	V	V	V	V
	VR		V	V	V	V	V	V

Appendix - MT6235 Chip Function (3/8)

Baseband chip feature list			MT6226	MT6225	MT6228	MT6229	MT6230	MT6235
Audio	Digital music		V	V	V	V	V	V
	WT 64 tones		V	V	V	V	V	V
	AAC		V	V	V	V	V	V
	aacPlus		V	V	V	V	V	V
	CT aacPlus			V	V	V	V	V
	CT aacPlusv2			V	V	V	V	V
	WMA				V	V	V	V
	G711				V	V	V	V
	G723.1				V	V	V	V
	G729				V	V	V	V
	AWB+				V	V	V	V
	Time stretch				V	V	V	V
	Audio EQ		V	V	V	V	V	V
	3D effect				V	V	V	V
	SBC		V	V	V	V	V	V
Memory system	Internal SRAM		2.2 Mb	384Kb	1 Mb	1 Mb	1 Mb	512 kb
	NAND boot			V	V	V	V	V
	External memory	Supply voltage	1.8/2.8V	1.8/2.8V	1.8/2.8V	1.8/2.8V	1.8/2.8V	1.8/2.8V
		Page mode	V	V	V	V	V	V
		Burst mode	*	V	Read	Read	Read	V
		Cellular RAM		V	V	V	V	V
		SDRAM		V	V	V	V	V
		Data width	8/16 bits	8/16 bits	8/16 bits	8/16 bits	8/16 bits	8/16 bits
		AD MUX		V				V
		Maximum size	64 MB	64 MB	64 MB	64 MB	64 MB	64 MB
		Device number	8	3	4	4	4	4

Appendix - MT6235 Chip Function (4/8)

Baseband chip feature list			MT6226	MT6225	MT6228	MT6229	MT6230	MT6235
Security	3GPP	A5/1	V	V	V	V	V	V
		A5/2	V	V	V	V	V	V
		A5/3		V		V	V	V
		GEA1	V	V	V	V	V	V
		GEA2	V	V	V	V	V	V
		GEA3		V		V	V	V
	Cipher	AES			V	V	V	
		DES/3DES			V	V	V	
	Hash	MD5			V	V	V	
		SHA-1			V	V	V	
	Secure boot		V	V	V	V	V	V
	Serial Link Authentication			V				V
	Secure flashing			V				V
	JTAG protection			V				V
	Chip UID		56-bit	64-bit	20-bit	20-bit	20-bit	315-bit
User Interface	Keypad	Row x Column	6x7	6x7	6x7	6x7	6x7	8x8
	PWM	Channel	2	2	2	2	2	4
	Alerter		1	1	1	1	1	0

Appendix - MT6235 Chip Function (5/8)

Baseband chip feature list			MT6226	MT6225	MT6228	MT6229	MT6230	MT6235
Connectivity	UART	Bps	921600	921600	921600	921600	921600	921k/3M
		Port	3	3	3	3	3	3
	USB	Speed	Full-speed	Full-speed	Full-speed	Full-speed	Full-speed	High-speed
		Controller	Device	Device	OTG	OTG	OTG	Device
	IrDA	SIR	V	V	V	V	V	V
		MIR			V	V	V	V
		FIR			V	V	V	V
	Bluetooth interface	Voice link	DAI/PCM	DAI/PCM	DAI/PCM	DAI/PCM	DAI/PCM	DAI/PCM
		Audio link	I2S	I2S	I2S	I2S	I2S	UART
	Wi-Fi interface		NFI	NFI	NFI	NFI	NFI	NFI
	SPI		1	1	1	1	1	1
	I2C		1	1	1	1	1	1
	I2S		1	1	1	1	1	1
Storage	Memory card	Supply voltage	2.8/3.3V	2.8/3.3V	2.8/3.3V	2.8/3.3V	2.8/3.3V	2.8/3.3V
	MMC	Version	3.3	3.3	3.3	3.3	3.3	3.3
	Memory Stick		V	V	V	V	V	V
	Memory Stick Pro		V	V	V	V	V	V
	SD		V	V	V	V	V	V
	NAND flash	Data width	8/16-bit	8/16-bit	8/16 bit	8/16 bit	8/16 bit	8/16-bit
		Page size	512/2k	512/2k	512/2k	512/2k	512/2k	512/2k
	SIM	Supply voltage	3V/1.8V (PMIC)	3V/1.8V (PMIC)	3V/1.8V (PMIC)	3V/1.8V (PMIC)	3V/1.8V (PMIC)	3V/1.8V
		USIM	V	V	V	V	V	V

Appendix - MT6235 Chip Function (6/8)

Baseband chip feature list			MT6226	MT6225	MT6228	MT6229	MT6230	MT6235
Graphics	LCM controller	Resolution	QVGA	170x220	CIF	CIF	CIF	CIF
		Parallel interface	8/9/16/18-bit	8/9/16/18-bit	8/9/16/18-bit	8/9/16/18-bit	8/9/16/18-bit	8/9/16/18-bit
		RGB interface						
		Serial interface	V	V	V	V	V	V
		High speed display interface						
		Blending layer	4	4	6	6	6	4
		Gamma correction	V			V	V	V
	2D	Resolution	16-bit		24-bit	24-bit	24-bit	24-bit
		SVG Tiny			V	V	V	V
	GIF decoder		V		V	V	V	
	PNG decoder				V	V	V	
Video	Digital video decoder	Profile	Simple		Simple	Simple	Simple	
		Level	0/1		0/1/2/3	0/1/2/3	0/1/2/3	
		Deblockfilter			V	V	V	
		Speed	QCIF@30fps		CIF@30fps	CIF@30fps	CIF@30fps	
	Digital video encoder	Profile	Simple		Simple	Simple	Simple	
		Level	0		0	0	0	
		Speed	QCIF@15fps		CIF@15fps	CIF@15fps	CIF@15fps	
	H.264 decoder	Profile						
		Speed						
	TV-out	TV-encoder			NTSC/PAL	NTSC/PAL		

Appendix - MT6235 Chip Function (7/8)

Baseband chip feature list			MT6226	MT6225	MT6228	MT6229	MT6230	MT6235
Image	Image input	Supply voltage	2.8/1.8V	2.8/1.8V	2.8V	2.8V	2.8V	2.8V/1.8V
		Bayer format	V		V	V	V	
		YUV format	V	V	V	V	V	V
		Data width	10-bit	8-bit	10-bit	10-bit	10-bit	8-bit
		Pixel clock input	V	V	V	V	V	V
		Sensor control	I2C	I2C	I2C	I2C	I2C	I2C
		High speed camera interface						
	Image signal processing	Pixels	VGA		3 M	3 M	1.3 M	
		Interpolation	5x5		7x7	7x7	7x7	
		Edge detection	5x5		5x3	5x5	5x5	
		Shading compensation	V		V	V	V	
		Defect compensation	V		V	V	V	
		Auto focus	V		V	V	V	
		Flash light	V		V	V	V	
		Image stabilization						
		Post filter	3x3		3x3	3x3	3x3	
	JPEG decoder	Baseline	V		V	V	V	
		Progressive	V		V	V	V	
	JPEG encoder	Baseline	V		V	V	V	
		YUV422	V		V	V	V	
		YUV420			V	V	V	
		JFIF			V	V	V	

Appendix - MT6235 Chip Function (8/8)

Baseband chip feature list			MT6226	MT6225	MT6228	MT6229	MT6230	MT6235
Mixed-Mode	APC-DAC		10-bit	10-bit	10-bit	10-bit	10-bit	10-bit
	AFC-DAC		13-bit	13-bit	13-bit	13-bit	13-bit	13-bit
	Voice-DAC		V	V	V	V	V	V
	Voice-ADC		V	V	V	V	V	V
	Audio-DAC	Channel	2	4	4	4	4	4
		Connection	AC	AC/DC	AC/DC	AC/DC	AC/DC	AC/DC
	Auxiliary-ADC	Channel	7	7	7	7	7	4(ext)+3(int)
		Resolution	10-bit	10-bit	10-bit	10-bit	10-bit	10-bit
	RX-ADC		14-bit	14-bit	14-bit	14-bit	14-bit	14-bit
	TX-DAC		10-bit	10-bit	10-bit	10-bit	10-bit	10-bit
	TVO-DAC				10-bit	10-bit	10-bit	
	FM radio	Input	Stereo	Stereo	Stereo	Stereo	Stereo	Stereo
		Recording	Mono	Mono	Mono	Mono	Mono	Mono
	Touch panel							V
Supply voltage	Core		1.8V	1.8V	1.2V	1.2V	1.2V	1.2V
	General I/O		2.8V	2.8V	2.8V	2.8V	2.8V	2.8V
Power management	LDO							11
	Buck SMPS							1
	Reset generator							V
	SIM level shifter							V
	Battery charger							5V
Package	Dimension		13x13	12x12	13x13	13x13	13x13	13x13
	Ball		296	264	314	314	314	362
	Ball pitch		0.65	0.65	0.65	0.65	0.65	0.5
	Compatibility		Series B	Series D	Series C	Series C	Series C	Series G
Process			0.16um LL	0.16um LP	0.13um LL+SP	0.13um LL+SP	0.13um LL+SP	0.11um LL+SP

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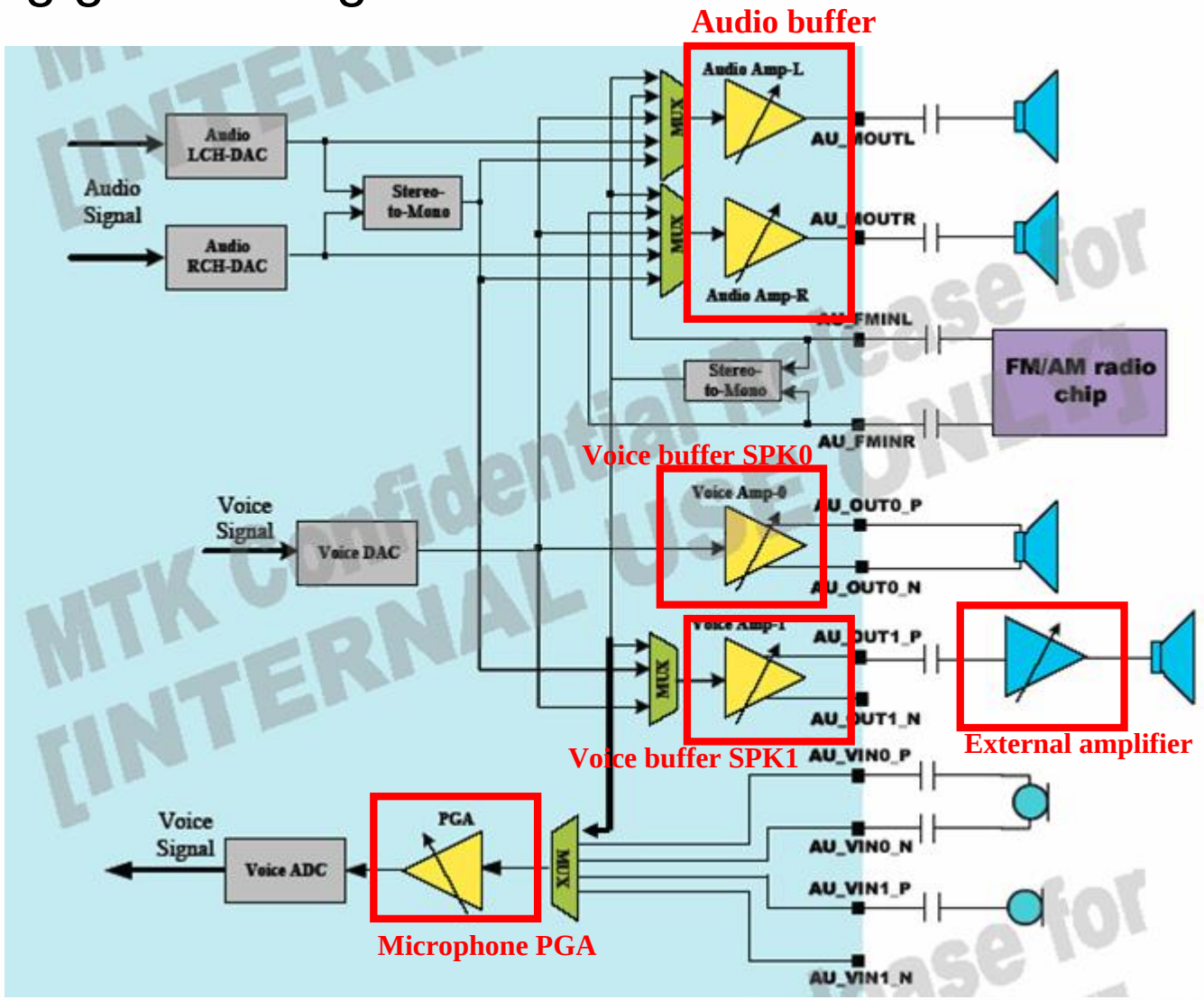
Appendix :
Common audio design notice

Outline

- Analog gain setting
- RC value
- PCB layout
- Audio feature
  - MP3 decoder
  - 3D surround effect
  - EQ 2.0
  - Audio AGC
  - Audio Compensation Filter
- For audio features, please refer to
  - L1_Audio_Design_and_Interface.pdf
  - Audio_Post-Processing_Interface_V1.13.pdf
  - Audio Customization v1.0.pdf

Audio block diagram

- Analog gain setting

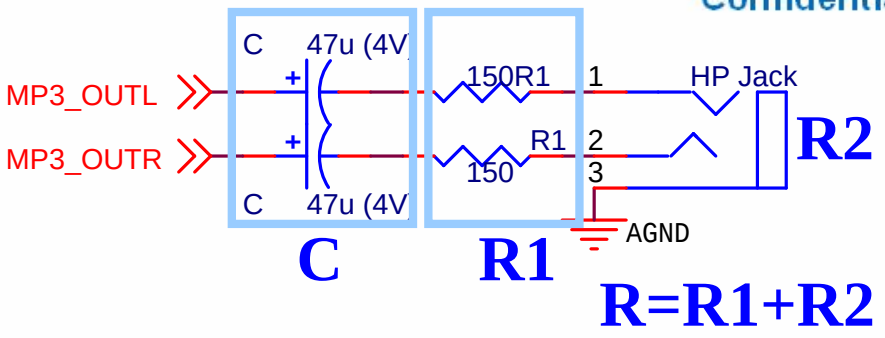


Audio buffer gain

- Analog gain setting
  - **LoudSPK mode**
    - **Audio buffer**
      - 112= -1dB
      - Positive gain results distortion
    - **External amplifier**
      - increasing external amplifier gain for louder volume
  - **Earphone mode**
    - **Audio buffer**
      - 112= -1dB
      - Positive gain results distortion
    - **External RC trade-off**

setting in engineering mode	audio Buffer [dB]	voice Buffer [dB]
240	23	8
224	20	6
208	17	4
192	14	2
176	11	0
160	8	-2
144	5	-4
128	2	-6
112	-1	-8
96	-4	-10
80	-7	-12
64	-10	-14
48	-13	-16
32	-16	-18
16	-19	-20
0	-22	-22

External RC value



- RC value on mp3_out path

1)Bandwidth: $$f_c = \frac{1}{2pRC}$$

2)Amplitude degradation: $$amplitude\ [dB] = 20\log\frac{R2}{R1+R2}$$

3)Larger resistance, better bass, smaller volume;

4)Larger capacitance, better bass, higher cost, larger PCB area.

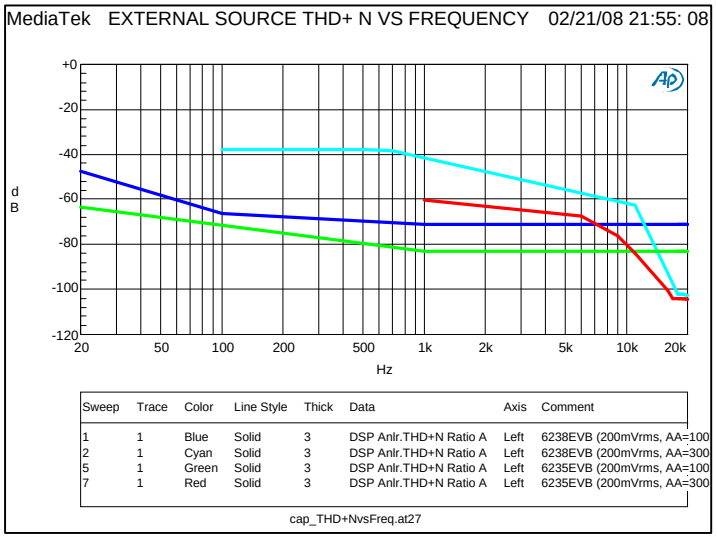
5)Pout < Earphone speaker rated power $$P_{out} = \frac{(V_{rms})^2}{R2}$$

6)example:

- (R1, C, Fc, Amplitude)
  - (470ohm, 22uF, 14Hz, -23.9dB)
  - (200ohm, 22uF, 31Hz, -17.2dB)
  - When C=22uF, earphone load R2=32 ohm,
  - Fcof R1=470ohm is lower 17Hz than Fcof R1=200ohm (31-14=17Hz)
  - Volume of R1=470ohm is smaller 6.7dB than that of R1=200ohm (-17.2+23.9=6.7dB)

External RC value

- **Different types of capacitors have different distortion.**
  - distortion: Tantalum cap. > MLCC X5R > MLCC Y5V
  - Don’t use MLCC Y5V in audio path/ mic0/ FM_IN
    - Capacitors’ THD+N vs. Frequency are showed as below:
    - green: X5R (+/-10%); Audio Precision Analyzer Rin=100kohm
    - red: X5R (+/-10%); Audio Precision Analyzer Rin=100kphm
    - blue: Y5V (+80%, -20%); Audio Precision Analyzer Rin=300ohm
    - cyan: Y5V (+80%, -20%); Audio Precision Analyzer Rin=300ohm

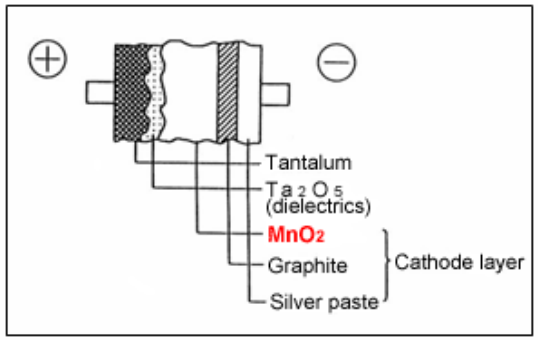


External RC value

- Tantalum capacitor
  - Can't be operated under reverse bias,
    - HP EINT can't be on earphone path.
  - Permissible reverse voltage:

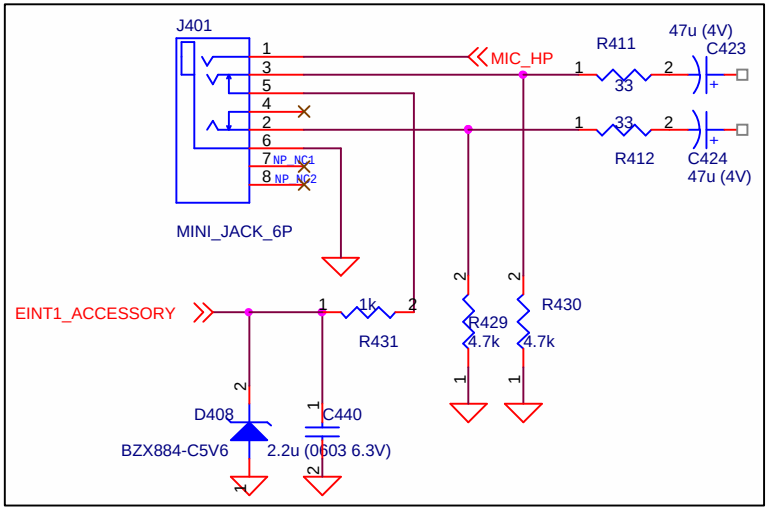
Ambient Temperature	25°C	55°C	85°C	125°C
Permissible Reverse Voltage	R.V. × 10% or 0.5V whichever is greater.	R.V. × 6%	R.V. × 3%	R.V. × 1%

  - The reason of damage by reverse voltage
    - Reverse voltage will damage Ta2O5,
    - After Ta2O5 is broken, there is large current passed through tantalum capacitor.



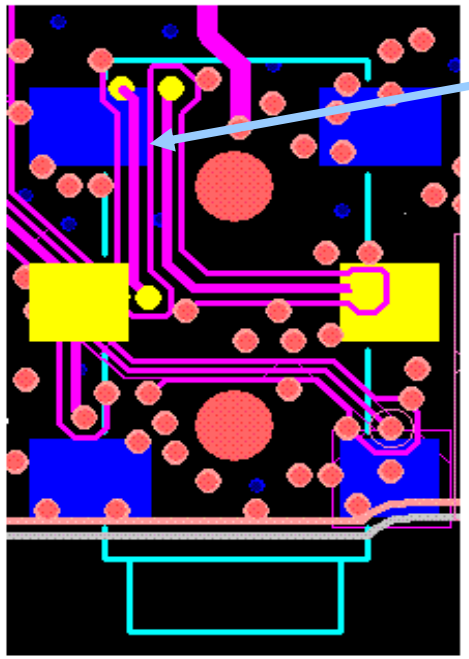
External RC value

- HP EINT suggestion
  - 18-pin I/O
    - An extra pin for HP EINT and accessory need a pull-low resister.
  - 6-pin earphone jack
    - Two extra pull-low resistors on CH-L/R



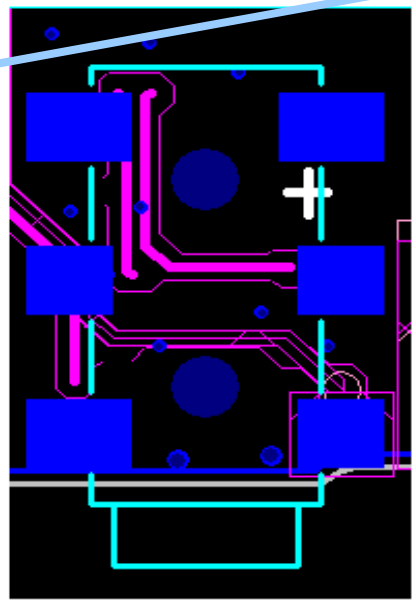
Audio traces

- Crosstalk issue
  - avoid CH-L and CH-R's signal interfering to each other
  - (1) PCB layout
    - **protected audio R & L stereo trace by GND separately.**



Superman29_V2

Crosstalk=70dB



Superman29_V1

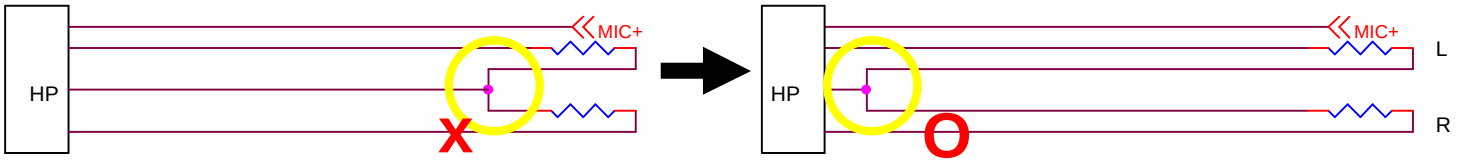
Superman29_V1

Crosstalk=45dB

In headset mode, please separate L/R channel and microphone trace by GND.

Audio traces

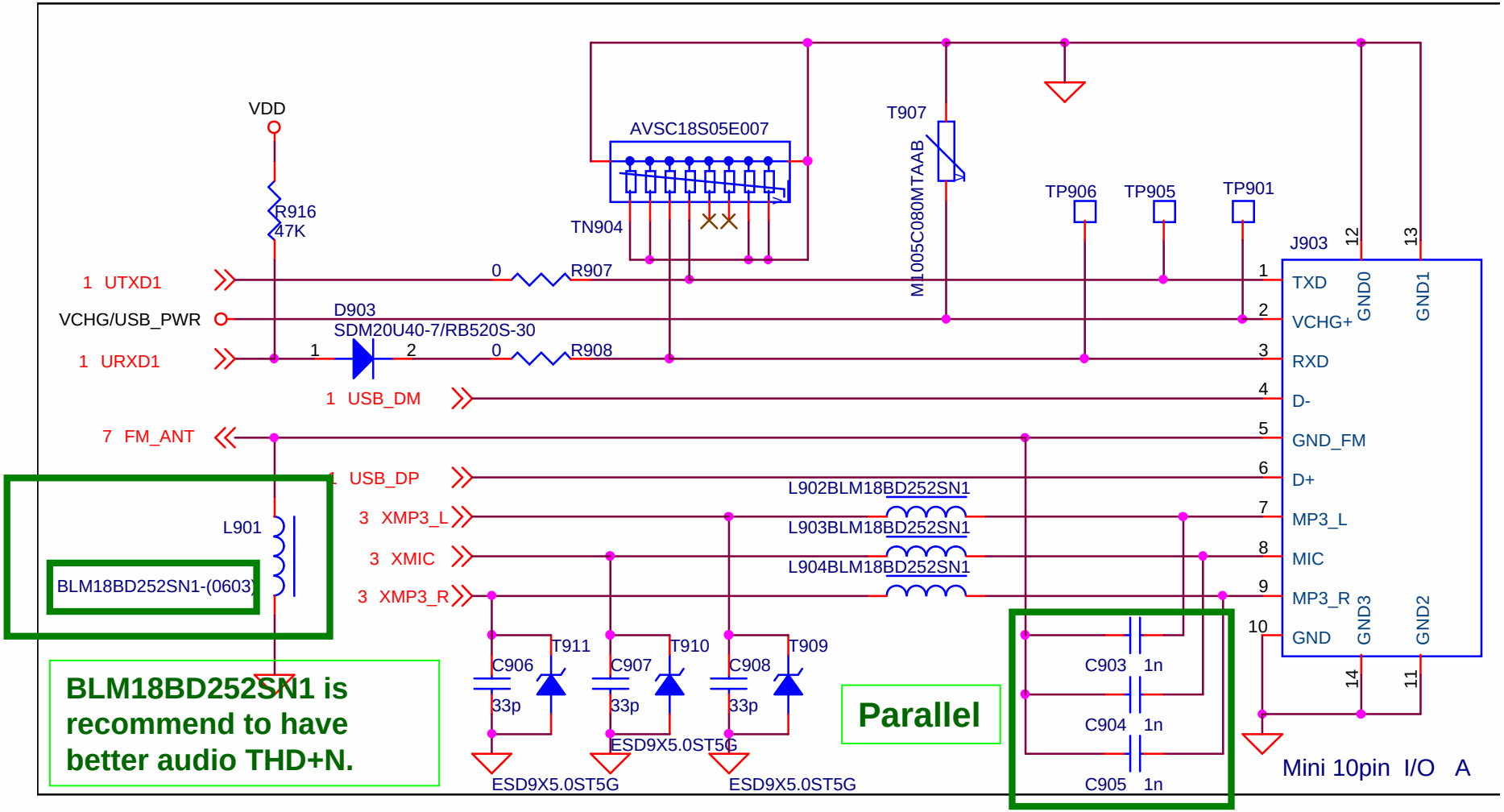
- Crosstalk issue
  - (2) earphone accessory:
    - Separated GND of CH-L and CH-R.
    - connect the GND of CH-L and CH-R at the end of earphone jack. Not connect the GND at earphone microphone.



  - (3) The bead at FM ANT on earphone path may degrade crosstalk about 15dB.
    - Choose bead with low DRC bead and good THD+N
    - It is a trade-off between FM feature and crosstalk performance.

I/O connector

I/O CONNECTOR



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Appendix :
MT6235 Memory Support Plan_20080624

MTK MVG (Memory Verification Group)

Entry-Level EDGE Phone

Segment	Entry-level VGA EDGE Phone	Entry-level 2M EDGE Phone
Platform	MT6235	MT6235
MCP	128+32 NOR+PSRAM	128+64 NOR+PSRAM
MCP Type	Multi-bank, Async.-page access	Multi-bank, Async.-page access
Memory P/N **(Week available)**	S71PL127NB0HFW4U **à** W08.27 S71PL127NB0HFW4B **à** W08.28 S71WS128NB0BFWAN **à** W08.28 PF38F3040M0Y0QE **à** W08.29 TV00570002ADGB **à** W08.29 K5L2731CAA **à** W08. 30 TV0057A002EAGD **à** W08.31 TV00579002GAGD **à** W08.31 M36L0T7050T3ZAQ M36L0R7050T2ZAQ LRS18D5 LRS18BK LRS18BL	S71PL127NC0HFW4U **à** W08.27 S71PL127NC0HFW4B **à** W08.28 S71WS128NC0BFWAM **à** W08.28 PF38F3050M0Y0QF **à** W08.29 PF38F3050L0YTQ2 **à** W08.29 K5L2763CAA **à** W0830 TV00670002ADGB **à** W08.31 TV0067A002DAGD **à** W08.31 TV00679002DAGD TV00679002CAGD M36L0R7060T1ZAQ LRS18D7 LRS18CA

*** For devices not included in the weeks available, please contact with MTK PM for status update.**

Feature-rich EDGE phone

Segment	GPS EDGE Phone	WIFI&GPS EDGE Phone
Platform	MT6235	MT6235
MCP	(512/1G)+256 NAND+SDRAM	(512/1G)+512 NAND+SDRAM
MCP Type	111/133/166 MHz SDR	111/133/166 MHz SDR
Memory P/N **(Week available)**	K5D12571CA-D090 (512+256) **à** W08.28 TY80009000FMGF10 (512+256) **à** W08.29 TY8000A000DMGF10 (1G+256) **à** W08.30 HYC0UEE0AF2P-3S60E (512+256) **à** W08.30 HowtehH-M3051301G-02 (512+256) **à** W08.32 K5D1G572CM-D075 (1G+256) HYC0UGE0MF2P-5SH0E (1G+256) HY5S5B6GLFP-6E (256Mb SDR) HYB18L256160BF-7.5 (256Mb SDR)	**TY9000A000GMGF (1G+512) à Passed!** K5D1G122CM-D075 (1G+512SDR) **à** W08.29 TY9000A000NMGF40 (1G+512) **à** W08.31 K5D1G12DCA-D090 (1G+512) **à** W08.31 HowtehH-M3061301G-02 (512+512) **à** W08.32 HYC0UGG0MF2P-5SH0E (1G+512) HYB18L512160BF-7.5 (512Mb SDR) HY5S7B6ALFP-H (512Mb SDR)

*** For devices not included in the weeks available, please contact with MTK PM for status update.**

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Appendix :
6235/6238/6239 LCM Design Guide

6235/38/39 LCM design guide

Ø Feature overview

	MT6235	MT6238	MT6239
Camera spec	2M 8bit Parallel IF YUV	3M 10 bit Parallel IF YUV, Bayer layer	5M 10bit Parallel IF YUV, Bayer layer
Mechanical Shutter	X	X	V
Auto Focus	X	V	V
XENON Flash	X	V	V
1.8V Camera IO voltage	X	V	V
LCM Spec	WQVGA 8,9,1618bit CPU IF	HVGA 8,9,1618bit CPU IF	HVGA 8,9,1618bit CPU IF
Intel 2.8V NOR+DDR memory	V_{note1}	V_{note1}	V_{note1}
Samsung 1.8V NAND+DDR memory	X_{note1}	V_{note1}	V_{note1}

Note1 : System memory share databuswith LCM interface

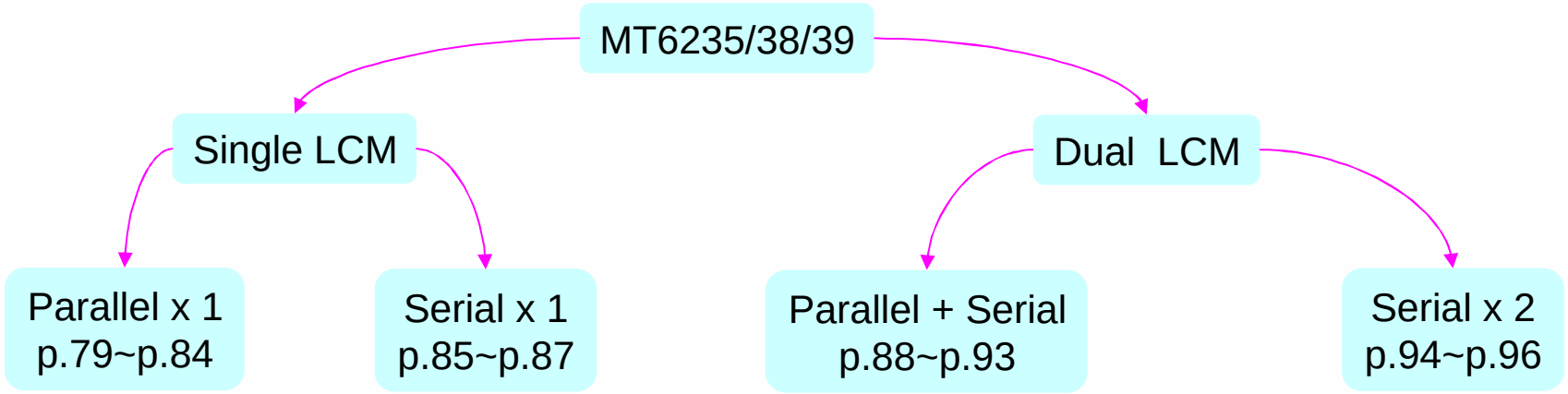
6235/38/39 LCM design guide

Ø LCM Guide map – HW ref. design selection

In this page, you will find the LCM hardware ref. design for

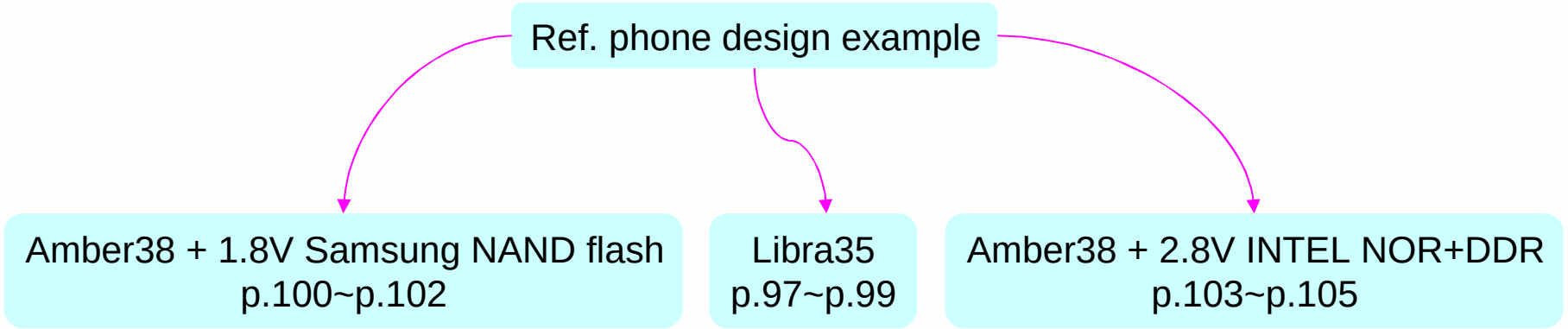
1. Single parallel LCM
2. Single serial LCM
3. Dual parallel + serial LCM
4. Dual serial LCM

over MT6235, MT6238/6239 Platform. (MT6239 pin definition is thesame as MT6238)



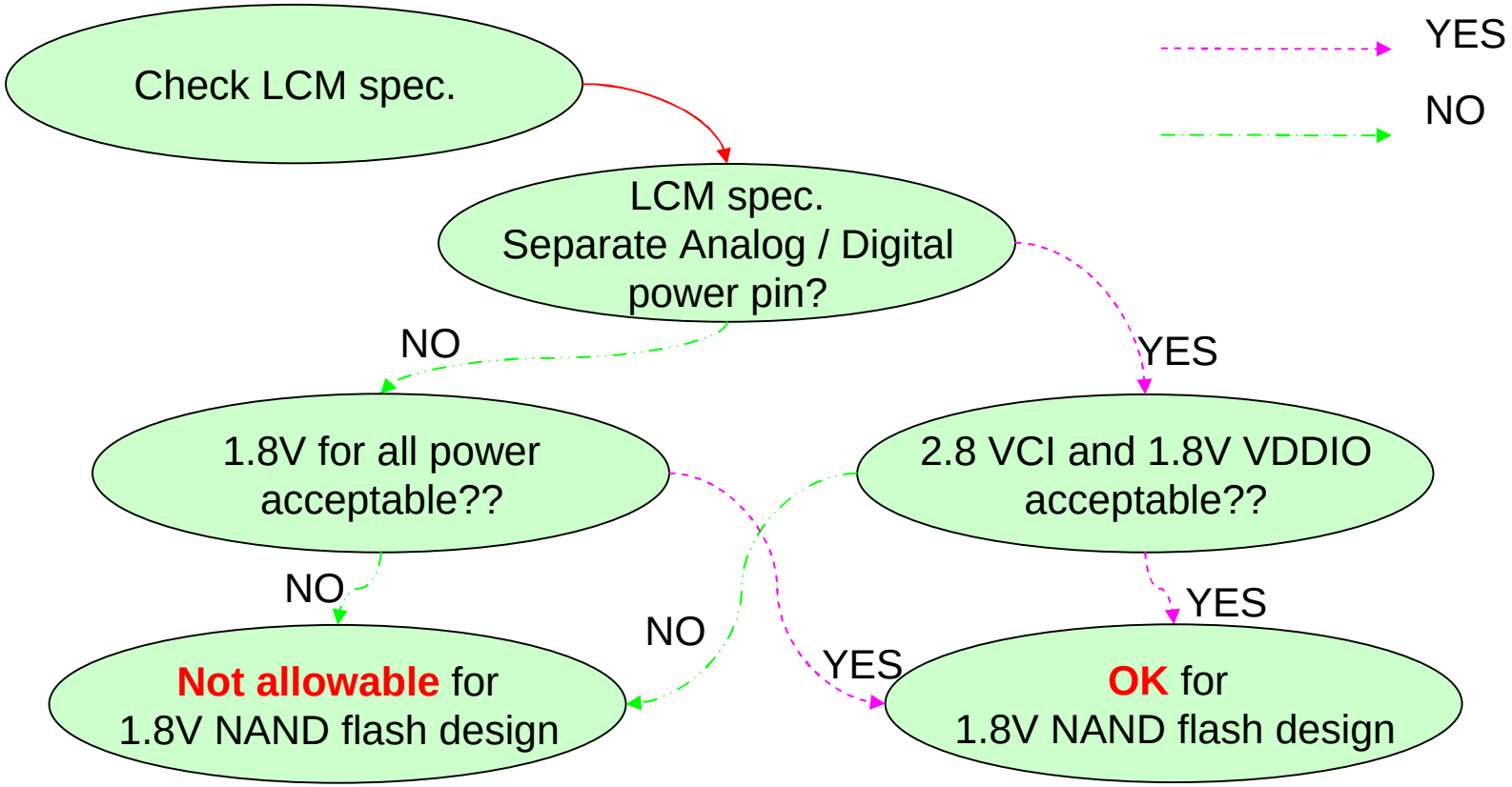
6235/38/39 LCM design guide

Ø LCM Guide map – Ref. phone design example
In this page, you will find the LCM hardware ref. design for
1. Libra35
2. Amber38 with 1.8V Samsung NAND flash
3. Amber38 with 2.8V Intel NOR+DDR



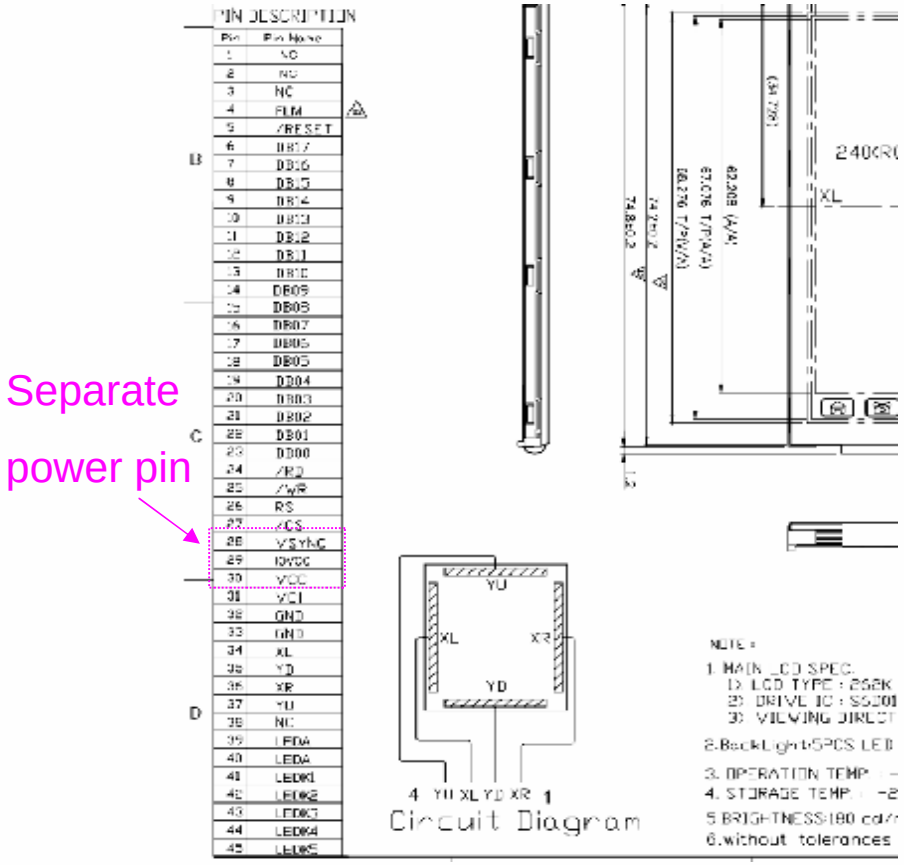
6235/38/39 LCM design guide

Ø LCM Guide map – 1.8V NAND flash compatibility
Because the LCM share databuswith NAND flash, LCM IO voltage need to be checked before NAND flash selection. In this page, you will find if LCM is compatible with 1.8V NAND flash.



6235/38/39 LCM design guide

- LCM Guide map – 1.8V NAND flash compatibility
  In this page, you will see an example of LCM IO **1.8V compatible case** which separates VCC (analog circuit) and IOVCC (IO voltage). Furthermore, IOVCC is 1.8V compatible.



wistron
Wistron Optronics Corp.

Model No.:T28WT7170	Rev : 11

24	/RD	A read strobe signal	I	
25	/WR	A write strobe signal	I	
26	RS	A register select signal	I	
27	/CS	A chip select signal	I	
28	VSYNC	Frame synchronizing signal for RGB interface In normal operation, Fix this pin at ground	I	
29	IOVCC	Power supply(1.65V~3.3V)	P	
30	VCC	VCC has Connected IOVCC in main FPC	P	
31	VCI	Power supply(2.5V~3.3V)	P	
32	GND	Ground	P	
33	GND	Ground	P	

IOVCC, VCC 1.8V acceptable

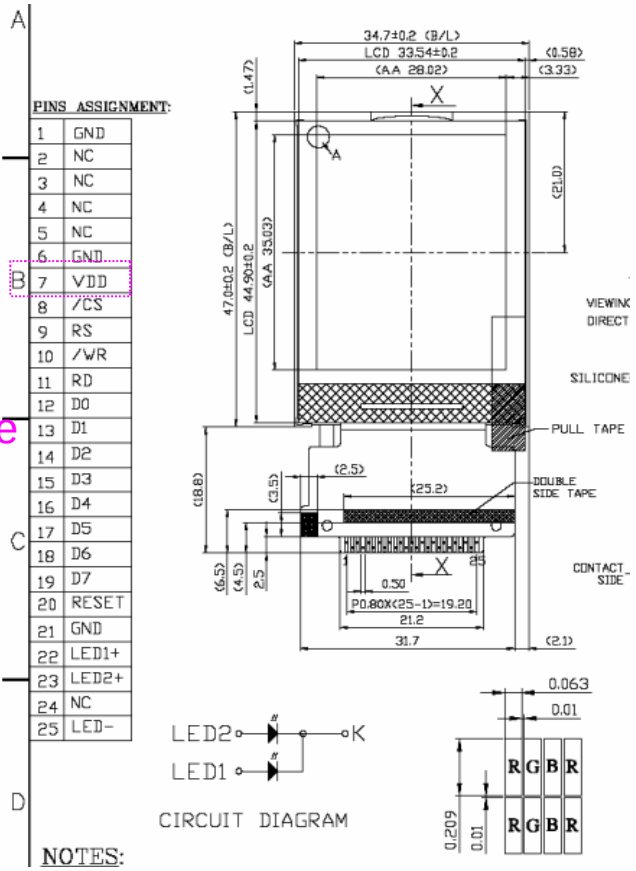
Where VCI=2.8V

6235/38/39 LCM design guide

Ø LCM Guide map – 1.8V NAND flash compatibility
In this page, you will see an example of LCM IO **1.8V incompatible case** which combines all power source to VDD pin. Furthermore, VDD **can't** support 1.8V

Non-separate power pin

Only one pin



5. **Electrical Specifications**

5.1 **Typical Electrical Characteristics**

At Ta=25±5°C, VDD=VDDIO=3.0V, GND=0V.

VDD,typical = 3V

Table 5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	VDD-GND		-	3.0	-	V
Supply voltage (LCD)	VLCD	Ta=-20°C, Note 1, VDD=3.0V	-	TBD	-	V
		Ta=+25°C, Note 1, VDD=3.0V	-	TBD	-	V
		Ta=+70°C, Note 1, VDD=3.0V	-	TBD	-	V
Supply Current (Logic & LCD)	IDD	All mode, VDD=3.0V	-	TBD	-	mA
Input high voltage	V_{IH}	VDD=3.0V	0.8VDDIO	-	VDDIO	V
Input low voltage	V_{IL}		GND	-	0.2VDDIO	V
Supply voltage of white LED backligh:	VLED	Forward current =30mA	3.0	3.2	3.4	V
Luminance of backligh:		Number of LED dies=2	3000	3500	-	cd/m²

Note (1): There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.

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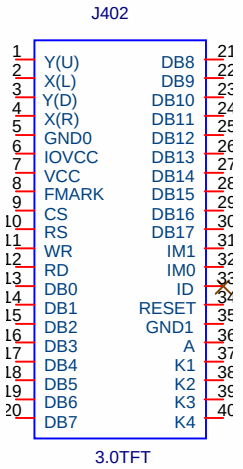
MT6235/38/39 Parallel IF LCM Ref. design

MT6235/38/39 Parallel IF LCM Ref. design

Ø All LCM control pins are BB dedicated pin (**don't connect to other pin!!**)

LCM pin	6235 pin map	6238 pin map	6239 pin map
WR (pin 11)	LWRB (pin AE14)	LWRB (pin AC9)	LWRB (pin AC9)
RD (pin 12)	LRDB (pin AD13)	LRDB (pin AB11)	LRDB (pin AB11)
CS (pin 9)	LPCE0B (pin U12)	LPCE0B (pin AD8)	LPCE0B (pin AD8)
RS (pin 10)	LPA0 (pin U13)	LPA0 (pin AE10)	LPA0 (pin AE10)
RESET (pin 33)	LRSTB (pin AC13)	LRSTB (pin AD9)	LRSTB (pin AD9)
FMARK (pin 8)	**LPTE (pin AE13)**	**LPTE (pin AC11)**	**LPTE (pin AC11)**
IOVCC (pin 6)	Follow VDD33_LCD(6235: pin AB13, AB17) (6238/39: pin U11, U12)		
VCC (pin 7)	VDD (2.8V)		

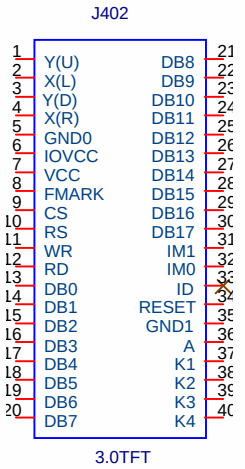


Parallel LCM pins

MT6235/38/39 Parallel IF LCM Ref. design

Ø All databusare NAND flash pins shared (**Notice interface pin number!!**)

LCM Pin	6235 pin map			
	8bit interface	9bit interface	16bit interface	18bit interface
DB17	x	x	x	NLD17 (pin AD14)
DB16	x	x	x	NLD16 (pin AC14)
DB15	x	x	NLD15 (pin AB14)	NLD15 (pin AB14)
DB14	x	x	NLD14 (pin U14)	NLD14 (pin U14)
DB13	x	x	NLD13 (pin AE15)	NLD13 (pin AE15)
DB12	x	x	NLD12 (pin AD15)	NLD12 (pin AD15)
DB11	x	x	NLD11 (pin AC15)	NLD11 (pin AC15)
DB10	x	x	NLD10 (pin AB15)	NLD10 (pin AB15)
DB9	x	x	NLD9 (pin AE16)	NLD9 (pin AE16)
DB8	x	NLD8 (pin AD16)	NLD8 (pin AD16)	NLD8 (pin AD16)
DB7	NLD7 (pin AC16)	NLD7 (pin AC16)	NLD7 (pin AC16)	NLD7 (pin AC16)
DB6	NLD6 (pin AB16)	NLD6 (pin AB16)	NLD6 (pin AB16)	NLD6 (pin AB16)
DB5	NLD5 (pin U16)	NLD5 (pin U16)	NLD5 (pin U16)	NLD5 (pin U16)
DB4	NLD4 (pin AE17)	NLD4 (pin AE17)	NLD4 (pin AE17)	NLD4 (pin AE17)
DB3	NLD3 (pin AD17)	NLD3 (pin AD17)	NLD3 (pin AD17)	NLD3 (pin AD17)
DB2	NLD2 (pin AC17)	NLD2 (pin AC17)	NLD2 (pin AC17)	NLD2 (pin AC17)
DB1	NLD1 (pin AE18)	NLD1 (pin AE18)	NLD1 (pin AE18)	NLD1 (pin AE18)
DB0	NLD0 (pin AD18)	NLD0 (pin AD18)	NLD0 (pin AD18)	NLD0 (pin AD18)

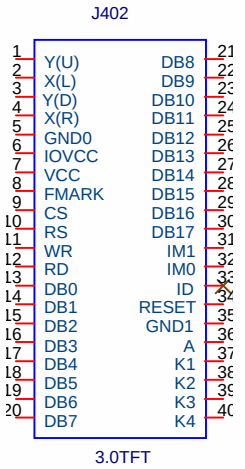


Parallel LCM pins

MT6235/38/39 Parallel + Serial IF LCM design

Ø All databusare NAND flash pins shared (**Notice interface pin number!!**)

LCM Pin	6238 / 6239 pin map			
	8bit interface	9bit interface	16bit interface	18bit interface
DB17	x	x	x	NLD17 (pin T12)
DB16	x	x	x	NLD16 (pin AE11)
DB15	x	x	NLD15 (pin AB13)	NLD15 (pin AB13)
DB14	x	x	NLD14 (pin AD10)	NLD14 (pin AD10)
DB13	x	x	NLD13 (pin T13)	NLD13 (pin T13)
DB12	x	x	NLD12 (pin AC10)	NLD12 (pin AC10)
DB11	x	x	NLD11 (pin U13)	NLD11 (pin U13)
DB10	x	x	NLD10 (pin AD11)	NLD10 (pin AD11)
DB9	x	x	NLD9 (pin AE12)	NLD9 (pin AE12)
DB8	x	NLD8 (pin T14)	NLD8 (pin T14)	NLD8 (pin T14)
DB7	NLD7 (pin AD12)	NLD7 (pin AD12)	NLD7 (pin AD12)	NLD7 (pin AD12)
DB6	NLD6 (pin AC12)	NLD6 (pin AC12)	NLD6 (pin AC12)	NLD6 (pin AC12)
DB5	NLD5 (pin AE13)	NLD5 (pin AE13)	NLD5 (pin AE13)	NLD5 (pin AE13)
DB4	NLD4 (pin AD13)	NLD4 (pin AD13)	NLD4 (pin AD13)	NLD4 (pin AD13)
DB3	NLD3 (pin AC13)	NLD3 (pin AC13)	NLD3 (pin AC13)	NLD3 (pin AC13)
DB2	NLD2 (pin AB14)	NLD2 (pin AB14)	NLD2 (pin AB14)	NLD2 (pin AB14)
DB1	NLD1 (pin U14)	NLD1 (pin U14)	NLD1 (pin U14)	NLD1 (pin U14)
DB0	NLD0 (pin AE14)	NLD0 (pin AE14)	NLD0 (pin AE14)	NLD0 (pin AE14)



Parallel LCM pins

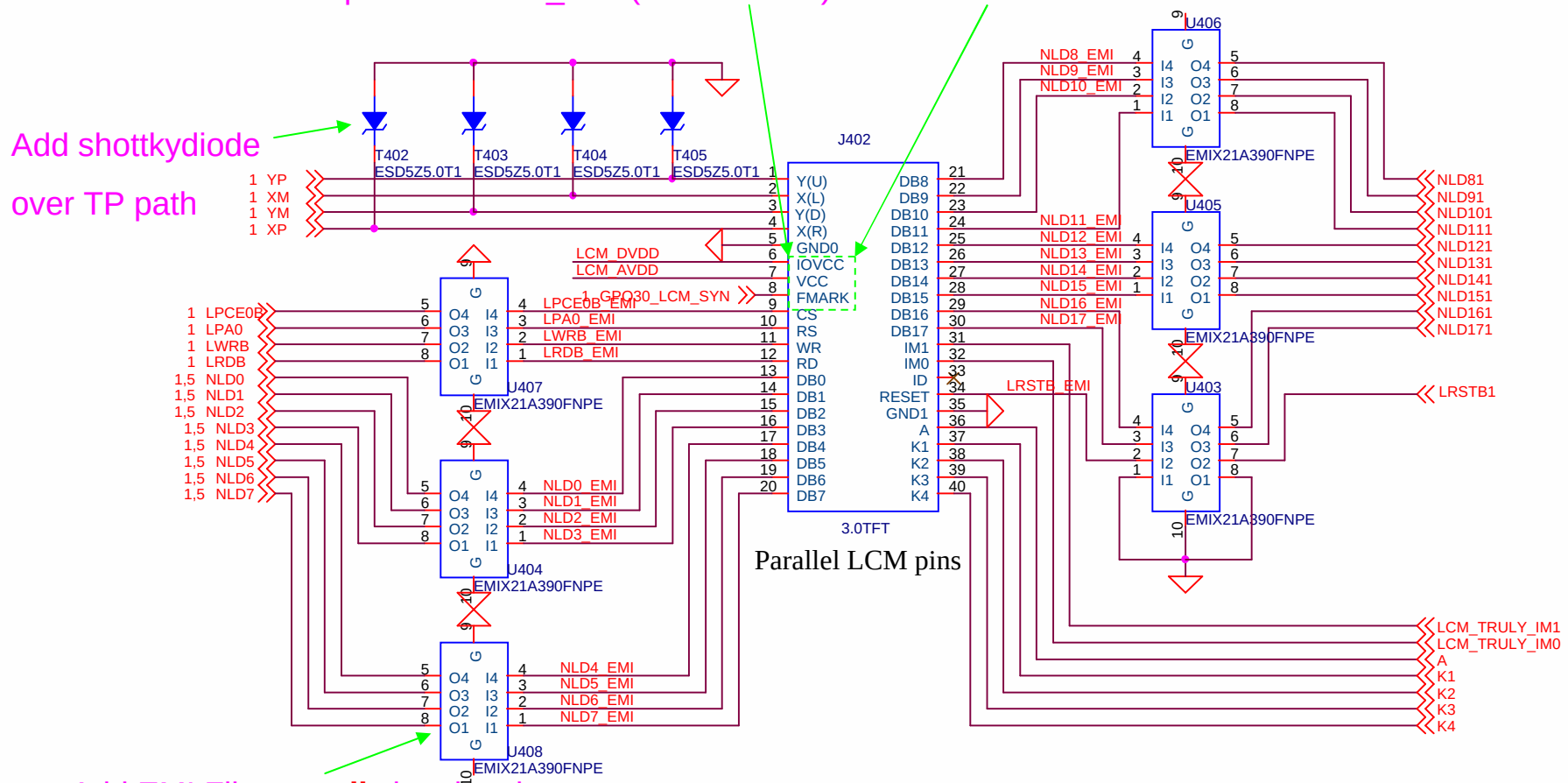
MT6235/38/39 Parallel IF LCM Ref. design

VCC connects to VDD(2.8V)

IOVCC == PMU power VDD33_LCD(2.8V or 1.8V)

FLM(FMARK) Connect to Dedicated LPTE

Add shottkydiode over TP path

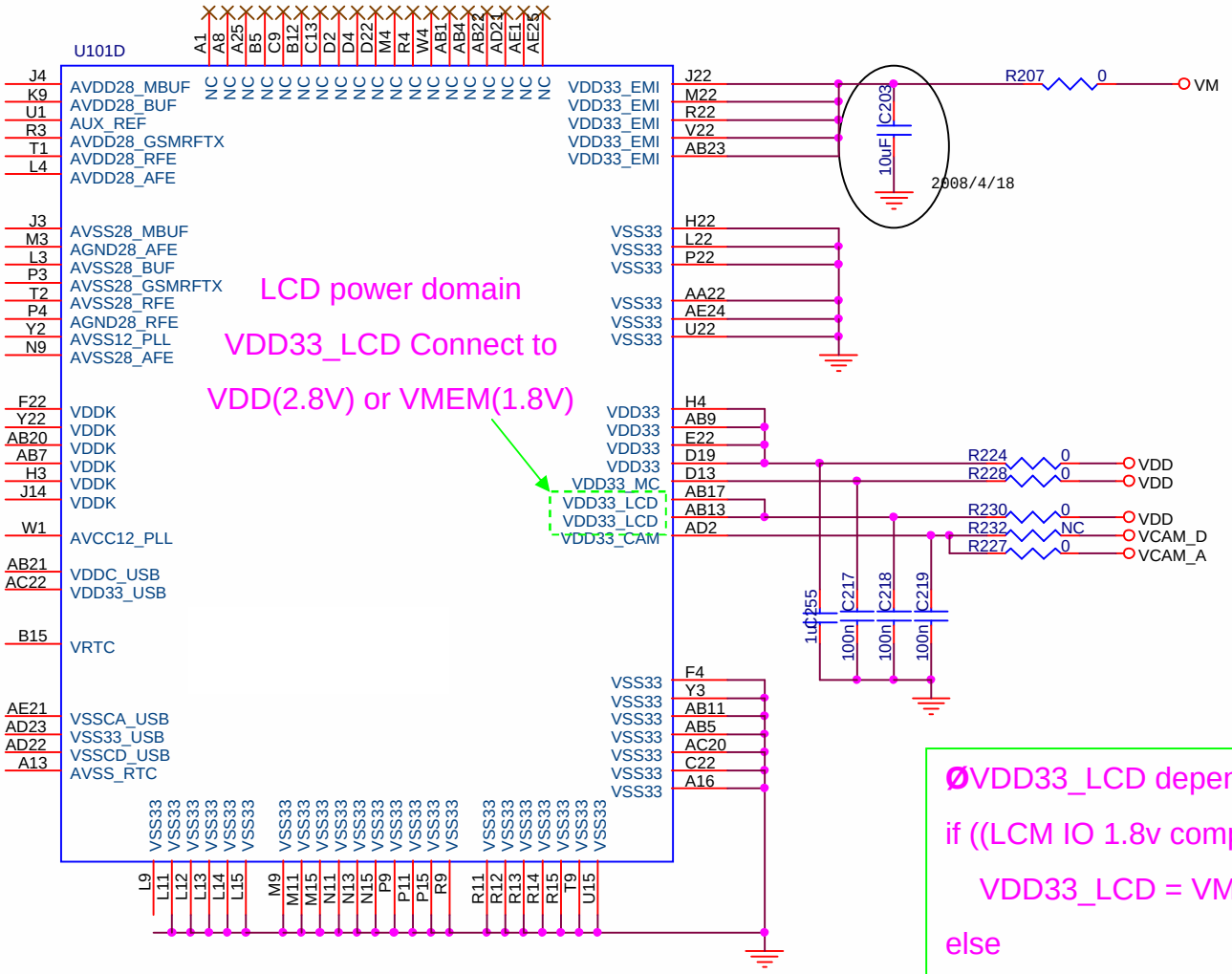


Parallel LCM pins

Add EMI Filter on **all** signal path

Between BB and LCM (close to LCM)

MT6235/38/39 Parallel IF LCM Ref. design



ØVDD33_LCD depends on NAND flash IO voltage

if ((LCM IO 1.8v compatible) && (NAND flash IO = 1.8V))

VDD33_LCD = VMEM /*1.8V*/

else

VDD33_LCD = VDD /*2.8V*/

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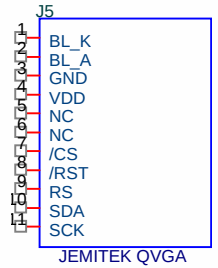
MT6235/38/39 Serial IF LCM Ref. design

MT6235/38/39 Serial IF LCM Ref. design

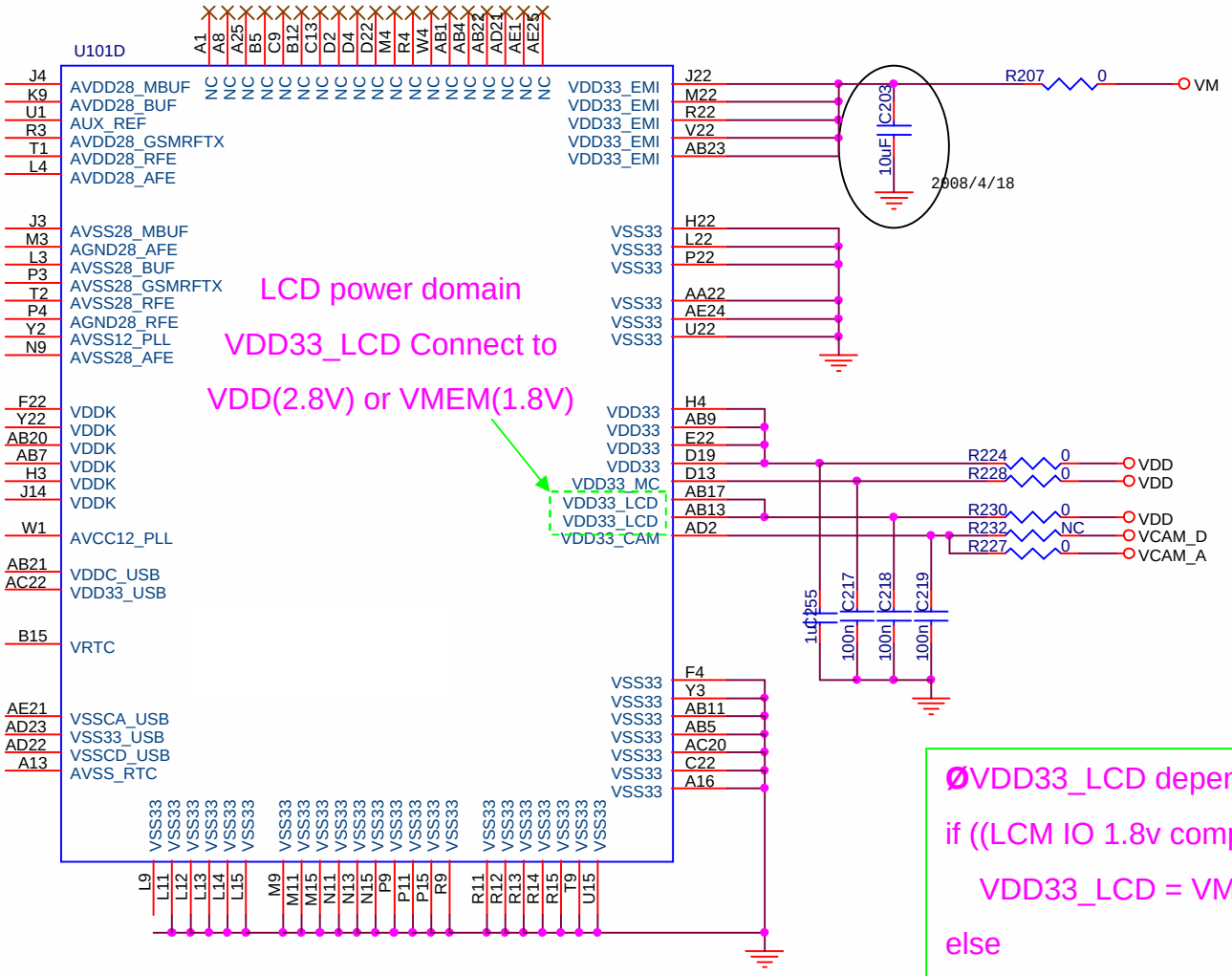
Ø All LCM control pins are BB dedicated pin (**don't connect to other pin!!**)

LCM pin	6235 pin map	6238 pin map	6239 pin map
SDA (pin 10)	LSDA (pin AD12)	LWRB (pin AC9)	LWRB (pin AC9)
SCK (pin 11)	LSCK (pin AC11)	LRDB (pin AB11)	LRDB (pin AB11)
/CS (pin 7)	LSCE0B (pin AE12)	LPCE0B (pin AD8)	LPCE0B (pin AD8)
RS (pin 9)	LSA0 (pin U11)	LPA0 (pin AE10)	LPA0 (pin AE10)
/RST (pin 8)	LRSTB (pin AC13)	LRSTB (pin AD9)	LRSTB (pin AD9)
VDD	Follow VDD33_LCD(6235: pin AB13, AB17) (6238/39: pin U11, U12)		



Serial LCM pins

MT6235/38/39 Serial IF LCM Ref. design



ØVDD33_LCD depends on NAND flash IO voltage

if ((LCM IO 1.8v compatible) && (NAND flash IO = 1.8V))

VDD33_LCD = VMEM /*1.8V*/

else

VDD33_LCD = VDD /*2.8V*/

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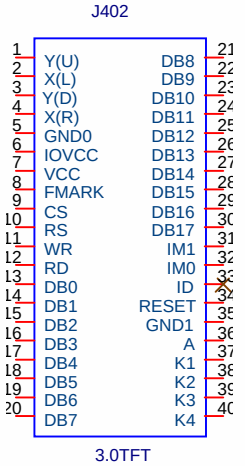
MT6235/38/39 Parallel + Serial IF LCM Ref. design

MT6235/38/39 Parallel + Serial IF LCM design

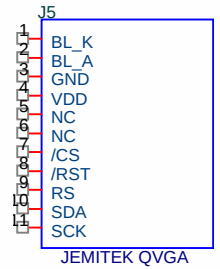
Ø All LCM control pins are BB dedicated pin (**don't connect to other pin!!**)

LCM pin	6235 pin map	6238 pin map	6239 pin map
WR (pin 11)	LWRB (pin AE14)	LWRB (pin AC9)	LWRB (pin AC9)
RD (pin 12)	LRDB (pin AD13)	LRDB (pin AB11)	LRDB (pin AB11)
CS (pin 9)	LPCE0B (pin U12)	LPCE0B (pin AD8)	LPCE0B (pin AD8)
RS (pin 10)	LPA0 (pin U13)	LPA0 (pin AE10)	LPA0 (pin AE10)
RESET (pin 33)	LRSTB (pin AC13)	LRSTB (pin AD9)	LRSTB (pin AD9)
FMARK (pin 8)	**LPTE (pin AE13)**	**LPTE (pin AC11)**	**LPTE (pin AC11)**
IOVCC (pin 6)	Follow VDD33_LCD(6235: pin AB13, AB17) (6238/39: pin U11, U12)		
VCC (pin 7)	VDD (2.8V)		



Parallel Main LCM

LCM pin	6235 pin map	6238 pin map	6239 pin map
SDA (pin 10)	LSDA (pin AD12)	LWRB (pin AC9)	LWRB (pin AC9)
SCK (pin 11)	LSCK (pin AC11)	LRDB (pin AB11)	LRDB (pin AB11)
/CS (pin 7)	LSCE0B (pin AE12)	LPCE0B (pin AD8)	LPCE0B (pin AD8)
RS (pin 9)	LSA0 (pin U11)	LPA0 (pin AE10)	LPA0 (pin AE10)
/RST (pin 8)	LRSTB (pin AC13)	LRSTB (pin AD9)	LRSTB (pin AD9)
VDD	Follow VDD33_LCD(6235: pin AB13, AB17) (6238/39: pin U11, U12)		

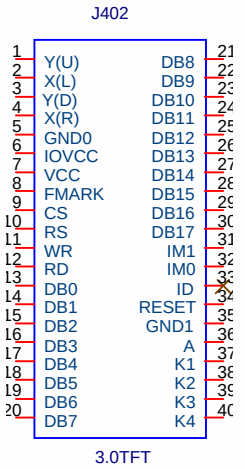


Serial Sub LCM

MT6235/38/39 Parallel + Serial IF LCM design

Ø All databusare NAND flash pins shared (**Notice interface pin number!!**)

LCM Pin	6235 pin map			
	8bit interface	9bit interface	16bit interface	18bit interface
DB17	x	x	x	NLD17 (pin AD14)
DB16	x	x	x	NLD16 (pin AC14)
DB15	x	x	NLD15 (pin AB14)	NLD15 (pin AB14)
DB14	x	x	NLD14 (pin U14)	NLD14 (pin U14)
DB13	x	x	NLD13 (pin AE15)	NLD13 (pin AE15)
DB12	x	x	NLD12 (pin AD15)	NLD12 (pin AD15)
DB11	x	x	NLD11 (pin AC15)	NLD11 (pin AC15)
DB10	x	x	NLD10 (pin AB15)	NLD10 (pin AB15)
DB9	x	x	NLD9 (pin AE16)	NLD9 (pin AE16)
DB8	x	NLD8 (pin AD16)	NLD8 (pin AD16)	NLD8 (pin AD16)
DB7	NLD7 (pin AC16)	NLD7 (pin AC16)	NLD7 (pin AC16)	NLD7 (pin AC16)
DB6	NLD6 (pin AB16)	NLD6 (pin AB16)	NLD6 (pin AB16)	NLD6 (pin AB16)
DB5	NLD5 (pin U16)	NLD5 (pin U16)	NLD5 (pin U16)	NLD5 (pin U16)
DB4	NLD4 (pin AE17)	NLD4 (pin AE17)	NLD4 (pin AE17)	NLD4 (pin AE17)
DB3	NLD3 (pin AD17)	NLD3 (pin AD17)	NLD3 (pin AD17)	NLD3 (pin AD17)
DB2	NLD2 (pin AC17)	NLD2 (pin AC17)	NLD2 (pin AC17)	NLD2 (pin AC17)
DB1	NLD1 (pin AE18)	NLD1 (pin AE18)	NLD1 (pin AE18)	NLD1 (pin AE18)
DB0	NLD0 (pin AD18)	NLD0 (pin AD18)	NLD0 (pin AD18)	NLD0 (pin AD18)

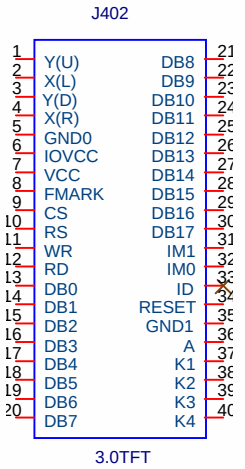


Parallel Main LCM

MT6235/38/39 Parallel + Serial IF LCM design

Ø All databusare NAND flash pins shared (**Notice interface pin number!!**)

LCM Pin	6238 / 6239 pin map			
	8bit interface	9bit interface	16bit interface	18bit interface
DB17	x	x	x	NLD17 (pin T12)
DB16	x	x	x	NLD16 (pin AE11)
DB15	x	x	NLD15 (pin AB13)	NLD15 (pin AB13)
DB14	x	x	NLD14 (pin AD10)	NLD14 (pin AD10)
DB13	x	x	NLD13 (pin T13)	NLD13 (pin T13)
DB12	x	x	NLD12 (pin AC10)	NLD12 (pin AC10)
DB11	x	x	NLD11 (pin U13)	NLD11 (pin U13)
DB10	x	x	NLD10 (pin AD11)	NLD10 (pin AD11)
DB9	x	x	NLD9 (pin AE12)	NLD9 (pin AE12)
DB8	x	NLD8 (pin T14)	NLD8 (pin T14)	NLD8 (pin T14)
DB7	NLD7 (pin AD12)	NLD7 (pin AD12)	NLD7 (pin AD12)	NLD7 (pin AD12)
DB6	NLD6 (pin AC12)	NLD6 (pin AC12)	NLD6 (pin AC12)	NLD6 (pin AC12)
DB5	NLD5 (pin AE13)	NLD5 (pin AE13)	NLD5 (pin AE13)	NLD5 (pin AE13)
DB4	NLD4 (pin AD13)	NLD4 (pin AD13)	NLD4 (pin AD13)	NLD4 (pin AD13)
DB3	NLD3 (pin AC13)	NLD3 (pin AC13)	NLD3 (pin AC13)	NLD3 (pin AC13)
DB2	NLD2 (pin AB14)	NLD2 (pin AB14)	NLD2 (pin AB14)	NLD2 (pin AB14)
DB1	NLD1 (pin U14)	NLD1 (pin U14)	NLD1 (pin U14)	NLD1 (pin U14)
DB0	NLD0 (pin AE14)	NLD0 (pin AE14)	NLD0 (pin AE14)	NLD0 (pin AE14)



Parallel Main LCM

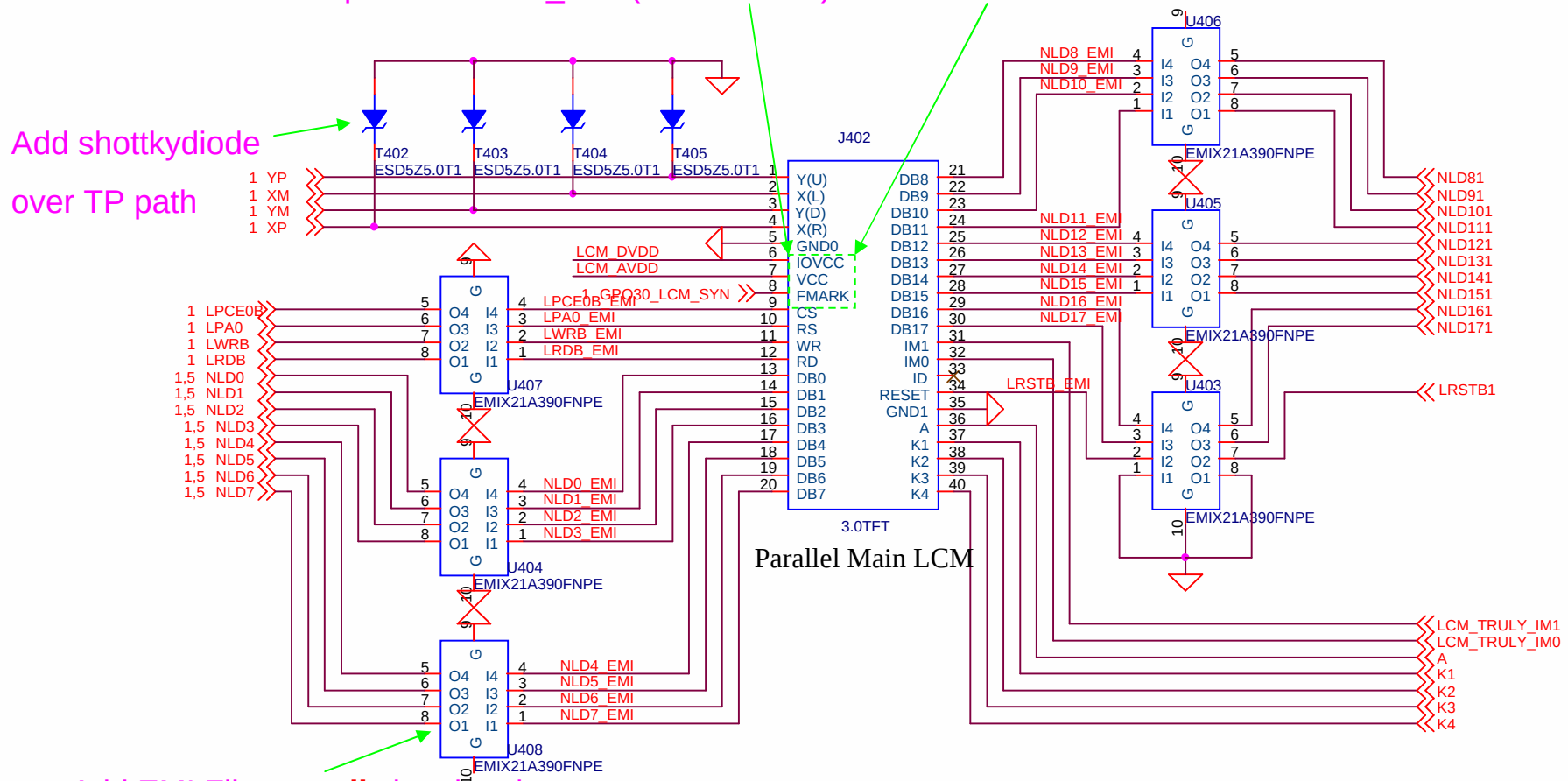
MT6235/38/39 Parallel + Serial IF LCM design

VCC connects to VDD(2.8V)

IOVCC == PMU power VDD33_LCD(2.8V or 1.8V)

FLM(FMARK) Connect to Dedicated LPTE

Add shottkydiode over TP path

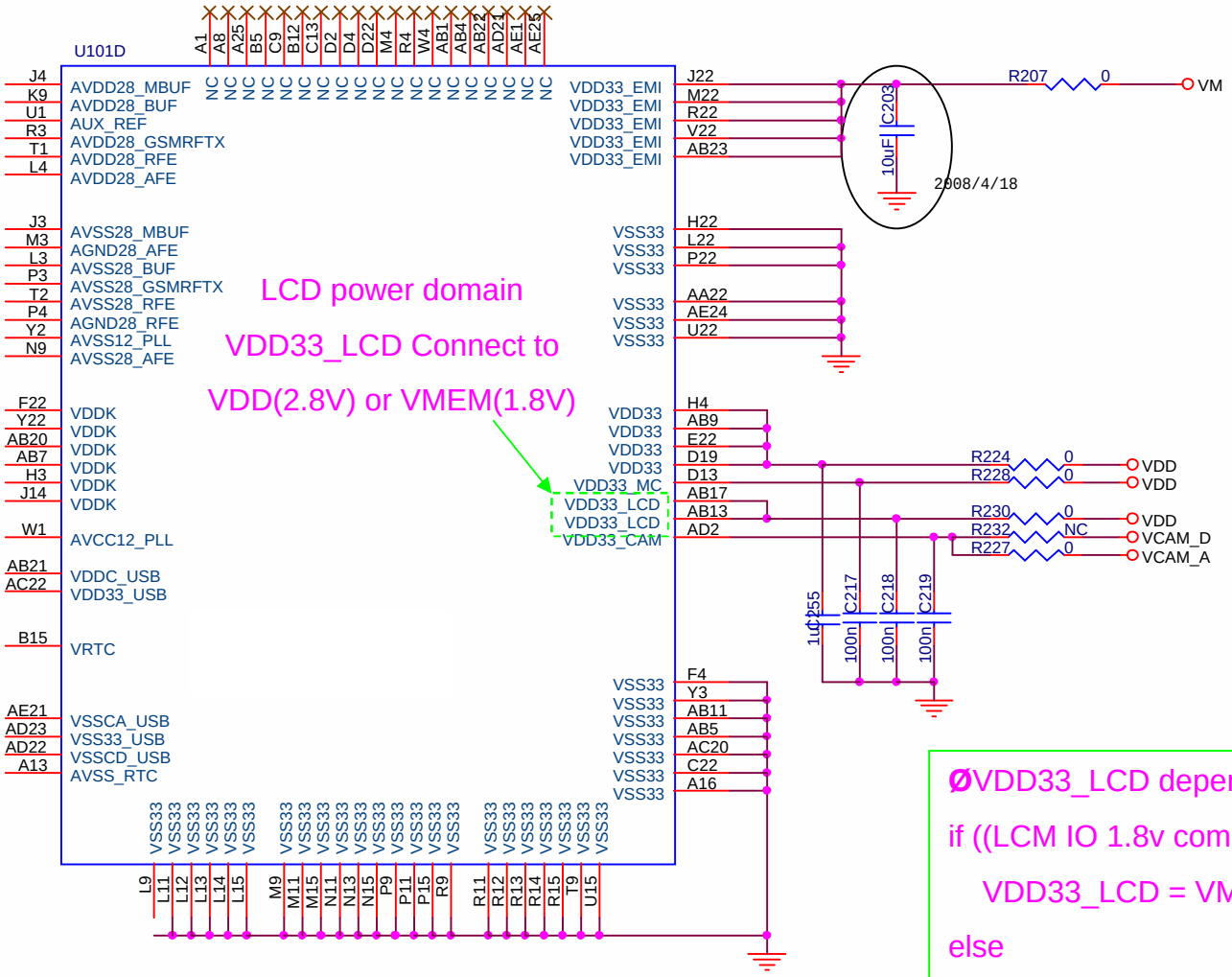


Parallel Main LCM

Add EMI Filter on **all** signal path

Between BB and LCM (close to LCM)

MT6235/38/39 Parallel + Serial IF LCM design



ØVDD33_LCD depends on NAND flash IO voltage

if ((LCM IO 1.8v compatible) && (NAND flash IO = 1.8V))

VDD33_LCD = VMEM /*1.8V*/

else

VDD33_LCD = VDD /*2.8V*/

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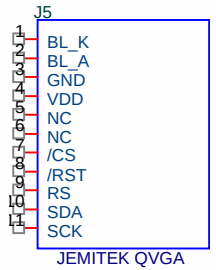
MT6235/38/39 Serial x2 IF LCM Ref. design

MT6235/38/39 Serial x 2 IF LCM Ref. design

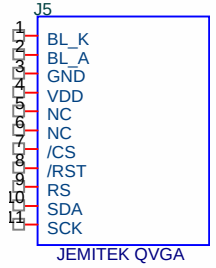
Ø All LCM control pins are BB dedicated pin (**don't connect to other pin!!**)

LCM pin	6235 pin map	6238 pin map	6239 pin map
SDA (pin 10)	LSDA (pin AD12)	LWRB (pin AC9)	LWRB (pin AC9)
SCK (pin 11)	LSCK (pin AC11)	LRDB (pin AB11)	LRDB (pin AB11)
/CS (pin 7)	**LSCE0B (pin AE12)**	**LPCE0B (pin AD8)**	**LPCE0B (pin AD8)**
RS (pin 9)	LSA0 (pin U11)	LPA0 (pin AE10)	LPA0 (pin AE10)
/RST (pin 8)	LRSTB (pin AC13)	LRSTB (pin AD9)	LRSTB (pin AD9)
VDD	Follow VDD33_LCD(6235: pin AB13, AB17) (6238/39: pin U11, U12)		



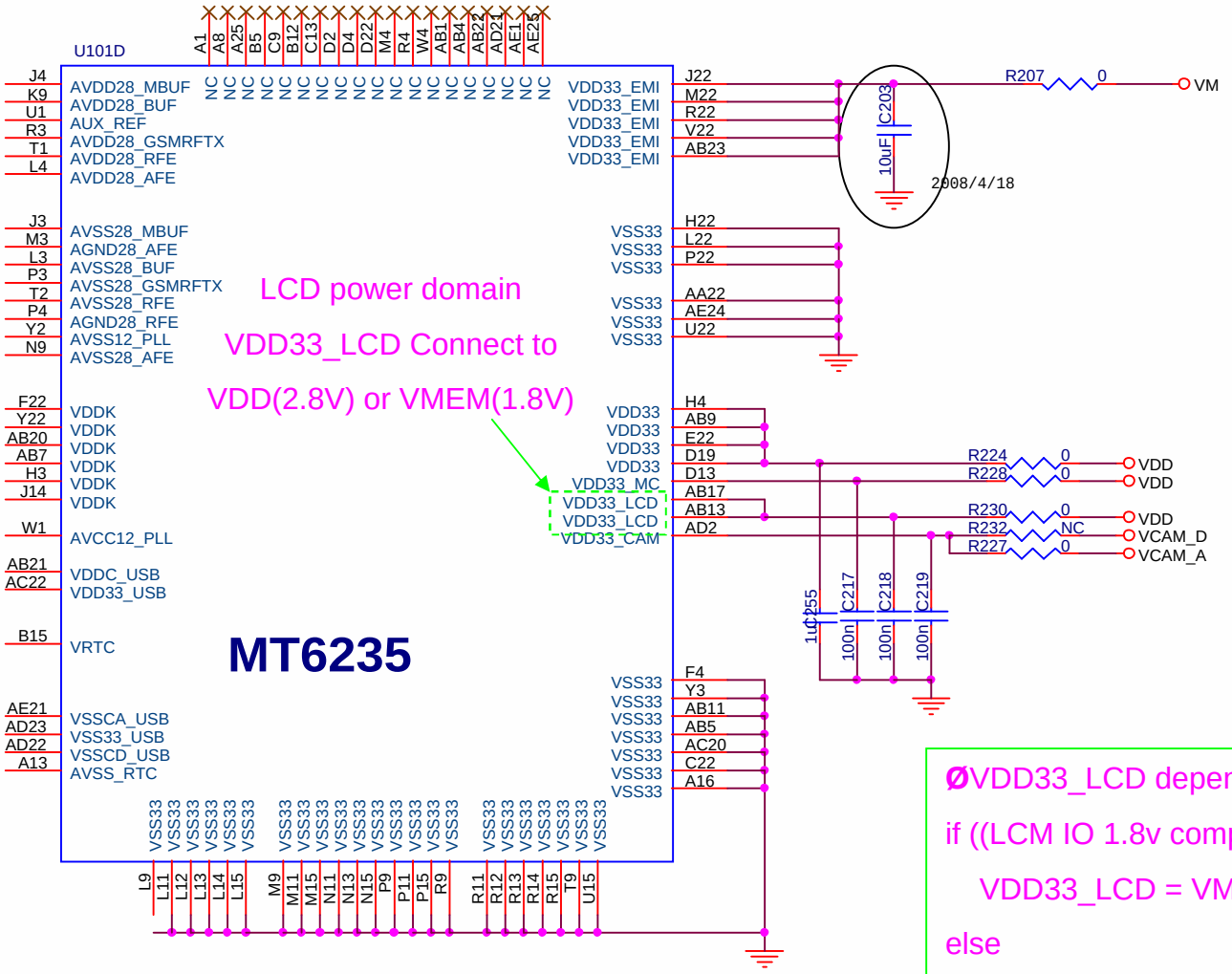
Serial Main LCM

LCM pin	6235 pin map	6238 pin map	6239 pin map
SDA (pin 10)	LSDA (pin AD12)	LWRB (pin AC9)	LWRB (pin AC9)
SCK (pin 11)	LSCK (pin AC11)	LRDB (pin AB11)	LRDB (pin AB11)
/CS (pin 7)	**LSCE1B (pin AC12)**	**LPCE1B (pin AC7)**	**LPCE1B (pin AC7)**
RS (pin 9)	LSA0 (pin U11)	LPA0 (pin AE10)	LPA0 (pin AE10)
/RST (pin 8)	LRSTB (pin AC13)	LRSTB (pin AD9)	LRSTB (pin AD9)
VDD	Follow VDD33_LCD(6235: pin AB13, AB17) (6238/39: pin U11, U12)		



Serial Sub LCM

MT6235/38/39 Serial x 2 IF LCM Ref. design



ØVDD33_LCD depends on NAND flash IO voltage

if ((LCM IO 1.8v compatible) && (NAND flash IO = 1.8V))

VDD33_LCD = VMEM /*1.8V*/

else

VDD33_LCD = VDD /*2.8V*/

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MEDIATEK

Libra35 LCM design note

Libra35 design note

VCC connects to VDD(2.8V)

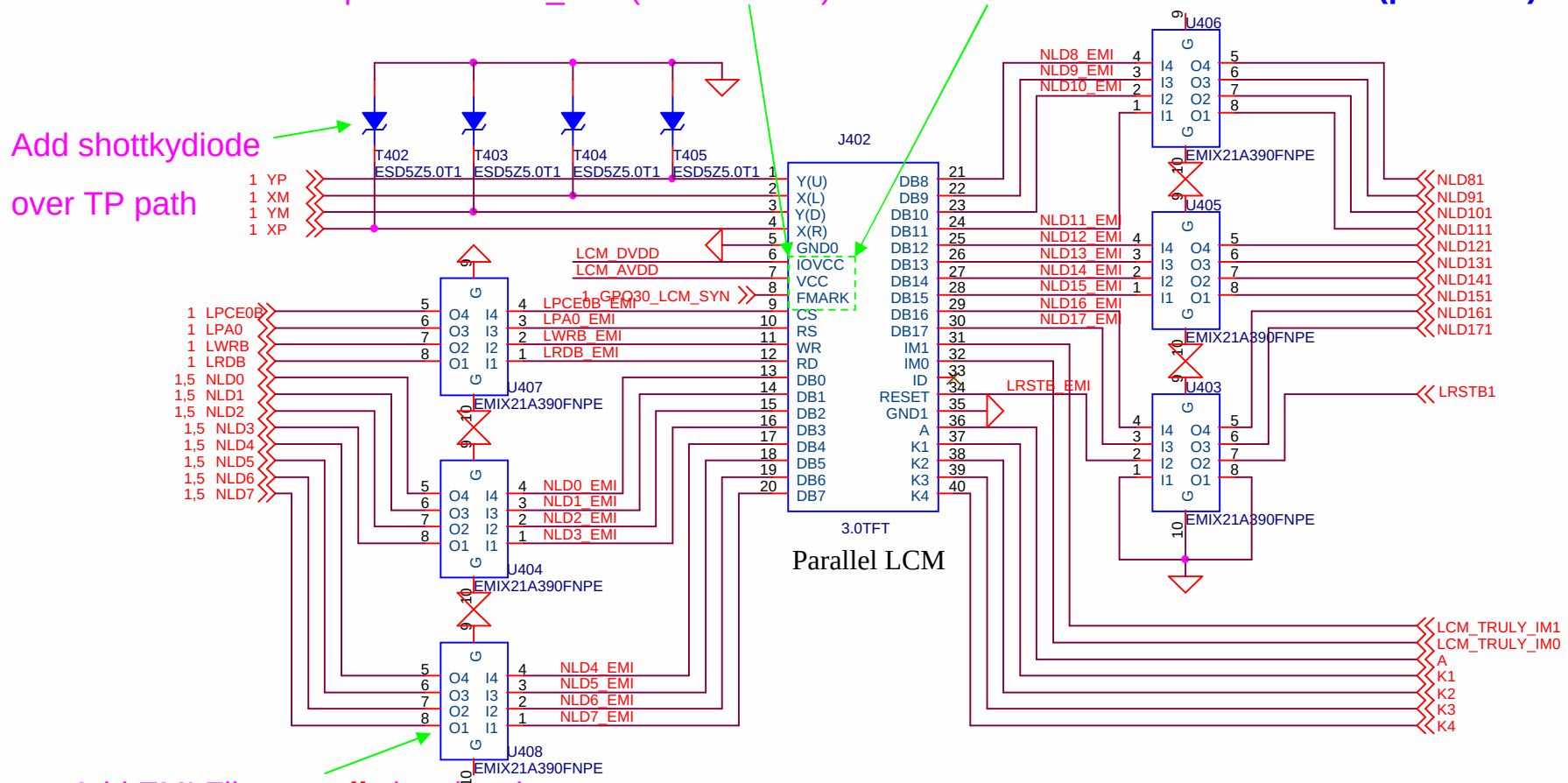
IOVCC == PMU power VDD33_LCD(2.8V or 1.8V)

FLM(FMARK) Connect to

Dedicated LPTE/GPIO30 (pin AE13)

Add shottkydiode

over TP path

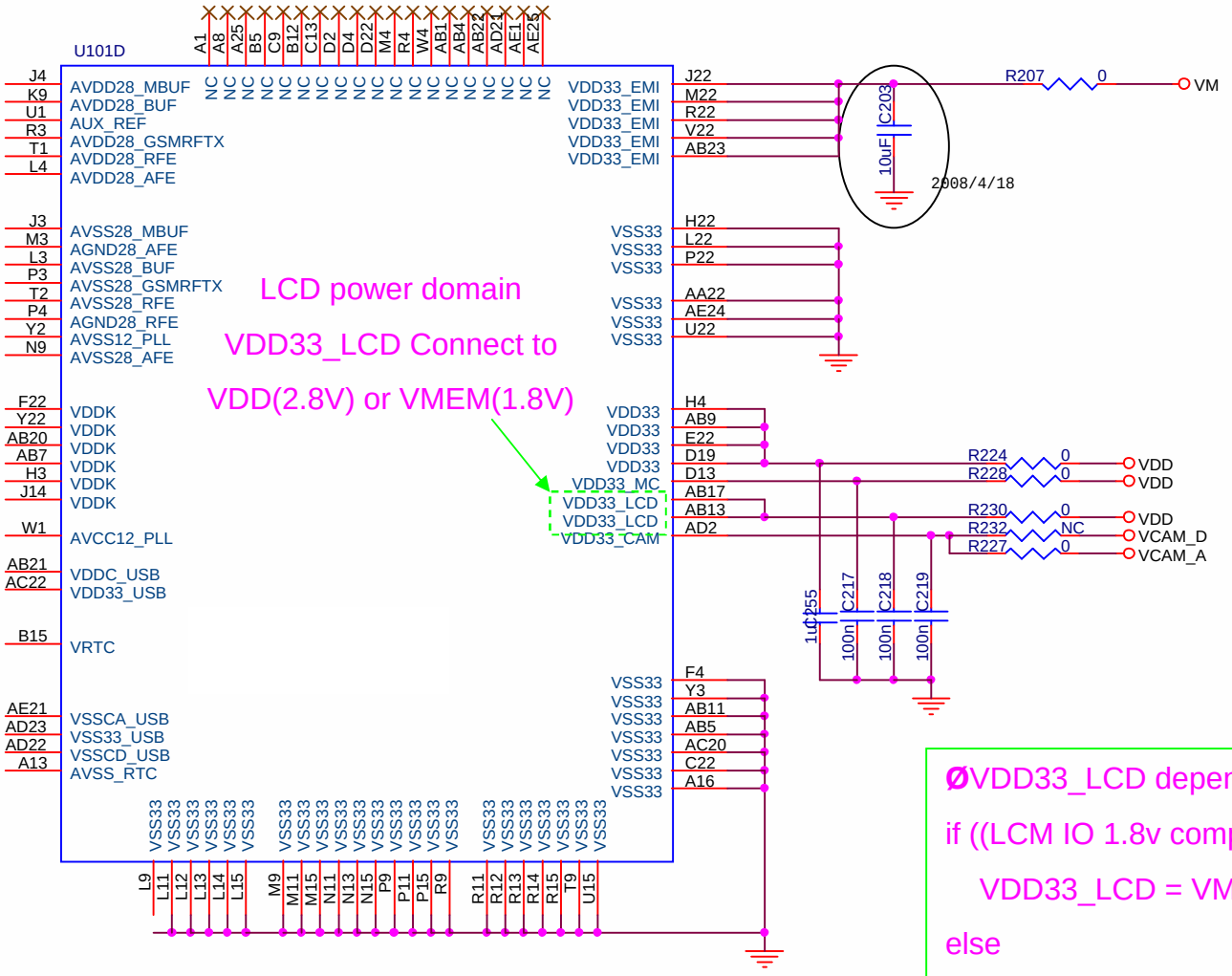


Parallel LCM

Add EMI Filter on **all** signal path

Between BB and LCM (close to LCM)

Libra35 design note



ØVDD33_LCD depends on NAND flash IO voltage

if ((LCM IO 1.8v compatible) && (NAND flash IO = 1.8V))

VDD33_LCD = VMEM /*1.8V*/

else

VDD33_LCD = VDD /*2.8V*/

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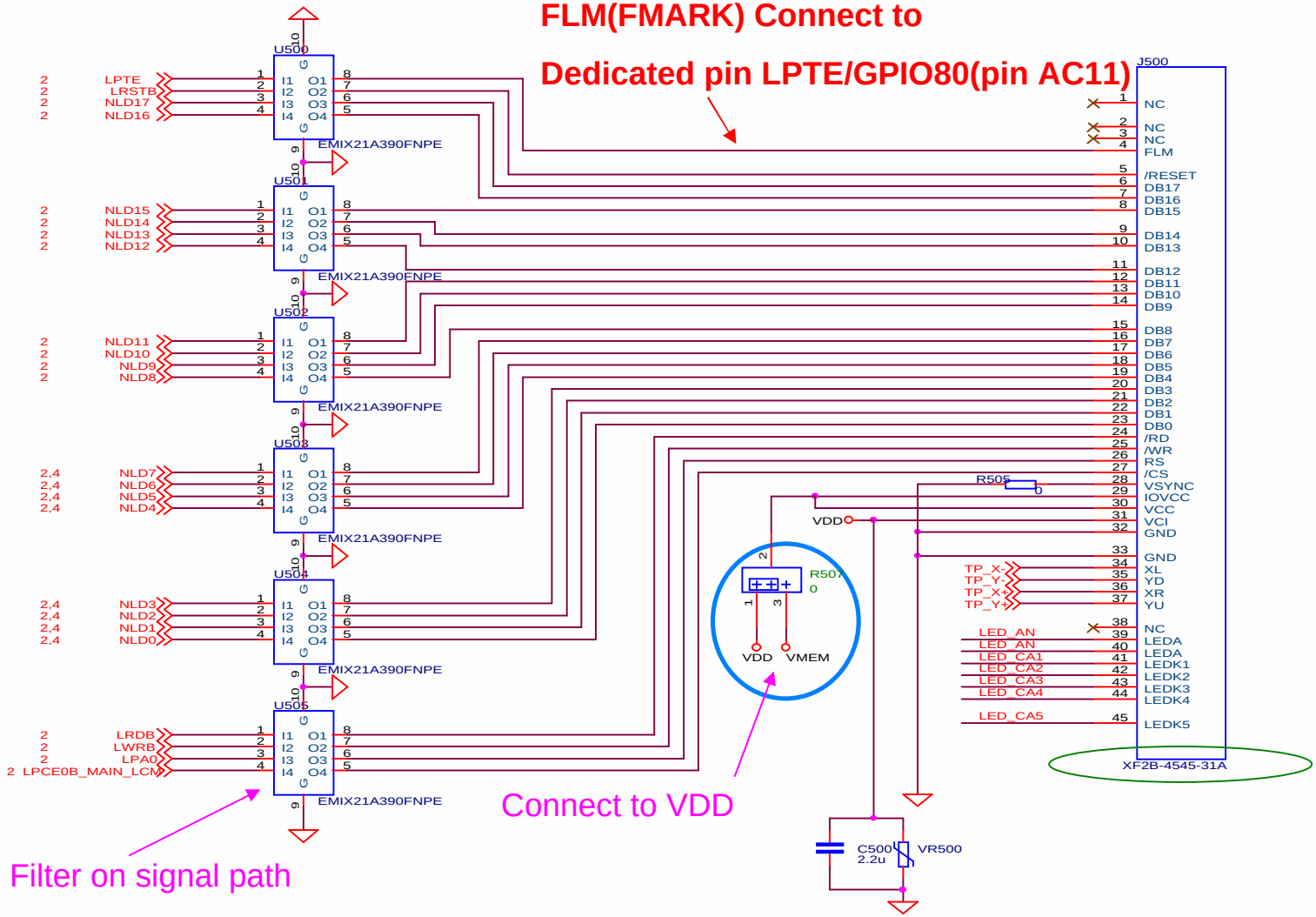
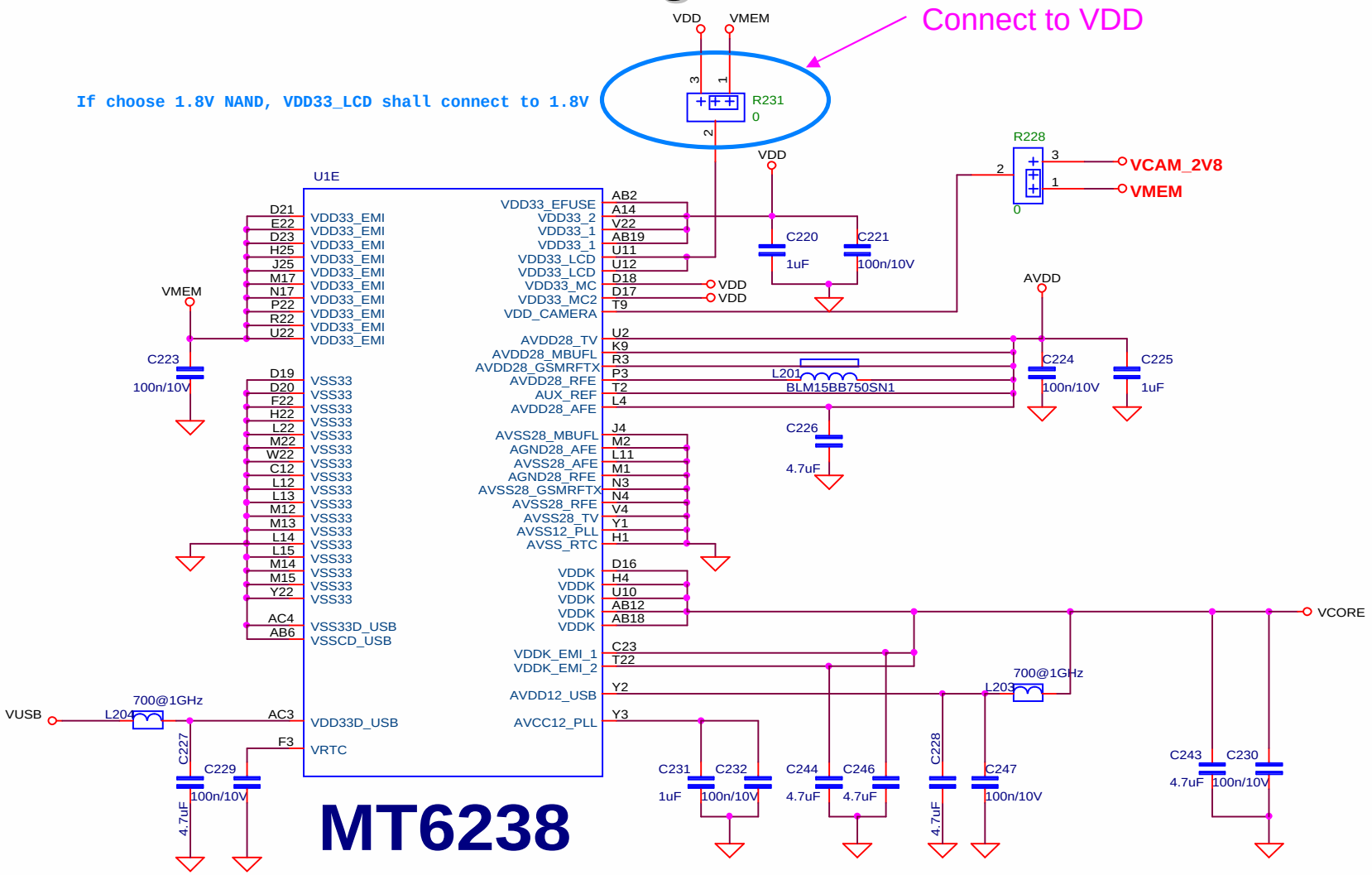
Amber38 design note
LCM module for
Intel 2.8V NOR+DDR MCP memory

Amber38 LCM Reference design



Amber38 PMU design note for 2.8V LCM IO



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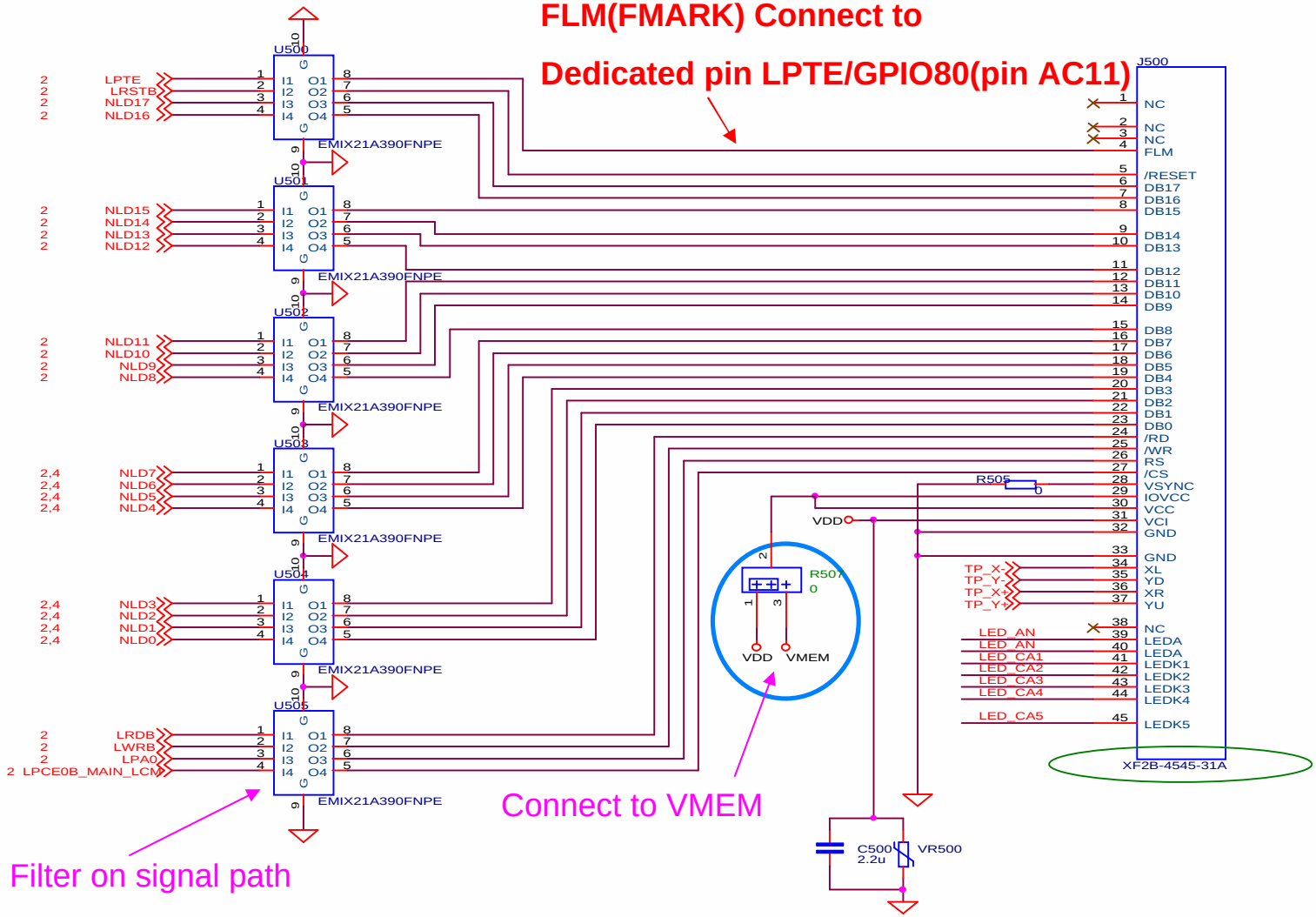
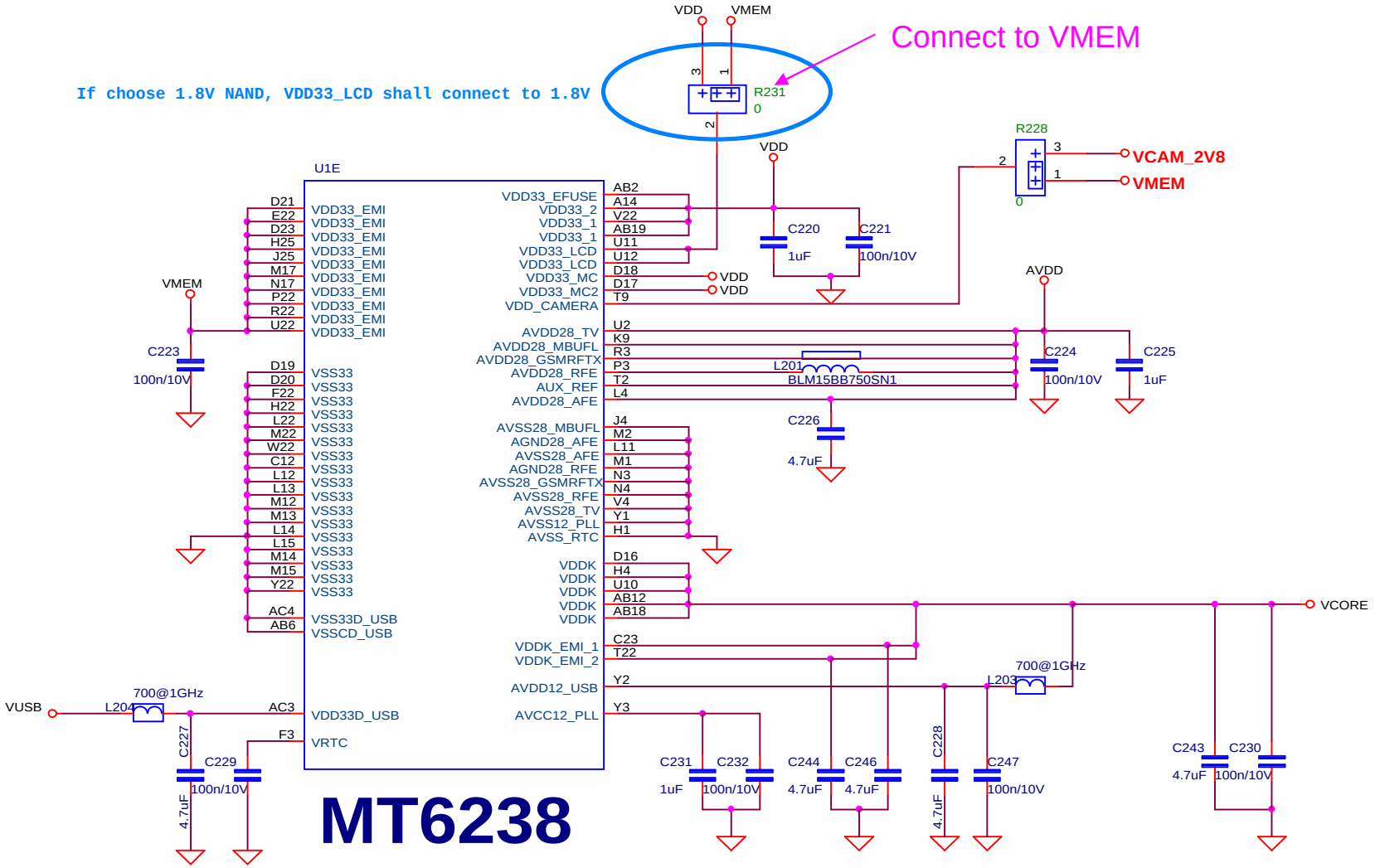
Amber38 design note
LCM module for
Samsung 1.8V NAND MCP memory

Amber38 LCM connector reference design



Amber38 PMU design note for 1.8V LCM IO



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