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MTK USB2.0/ OTG Design Guide V1.2

Schematics and Cable Design

2008/05/26

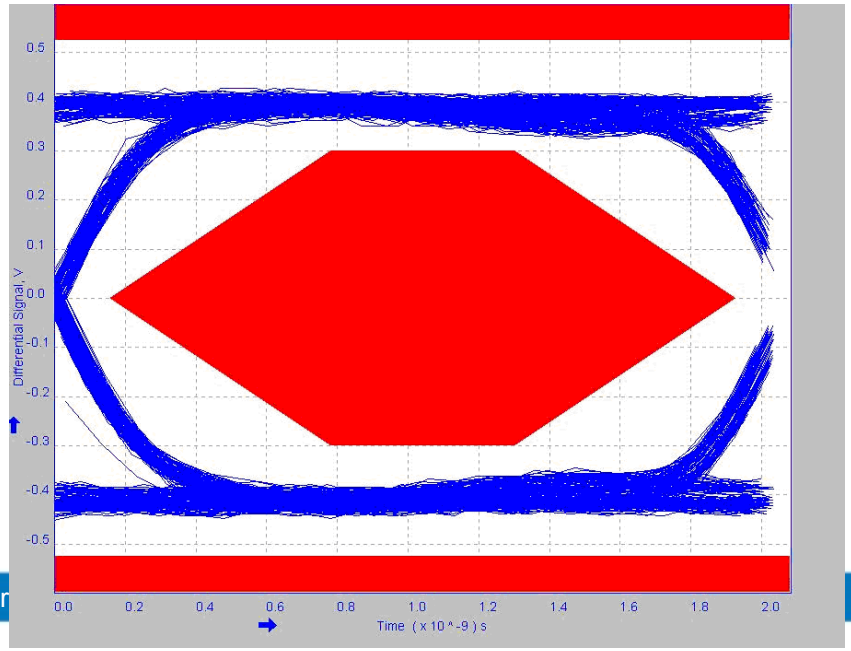
MediaTek Inc.

Outline

- Introduction
- MTK USB2.0 schematics design
- USB2.0 layout check list
- Case Study
- USB/ OTG cable design
  - Standard USB cable
  - Customized USB cable

MTK USB2.0 Solution Introduction

- This document introduces MTK USB2.0 design and some points for attention.
  - MTK USB2.0/ OTG device can operate at USB2.0 High-Speed (HS) mode (480Mb/s) and Full-Speed (FS) mode (12Mb/s).
- General HS eye diagram is shown as below. The output swing is differential 0.4V. Bad eye diagram will lead to certification fail or signal integrity problem.



Pin Definition (1/2)

- USB2.0 pin out description.
  - General pins

Pin	Symbol	Type	Description
1	PAD_USB_VBUS	IO	* Comparator used for detecting changes of VBUS voltage.
2	PAD_USB_DM	IO	USB serial differential bus (minus)
3	PAD_USB_DP	IO	USB serial differential bus (positive)
4	AVDD3_USB	VDD	Analog 3.3V supply
5	AVSS33_USB	GND	Analog 3.3V ground
6	PAD_USB_VRT	IO	Analog 5.1K reference resistor
7	AVDD12_USB	VDD	Analog 1.2V supply.
8	AVSS12_USB	GND	Analog 1.2V ground

  - Optional pins for external crystals

Pin	Symbol	Type	Description
9	PAD_USB_XTALI	IO	Reserved. Currently replaced by internal PLL.
10	PAD_USB_XTALO	IO	Reserved. Currently replaced by internal PLL.

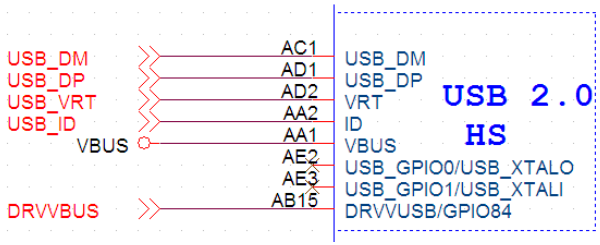
Pin Definition (2/2)

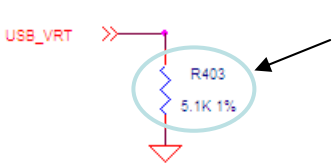
– Optional pins for supporting OTG

Pin	Symbol	Type	Description
11	PAD_USB_ID	IO	Optional function for USB OTG ID pin for detecting slave plug in.

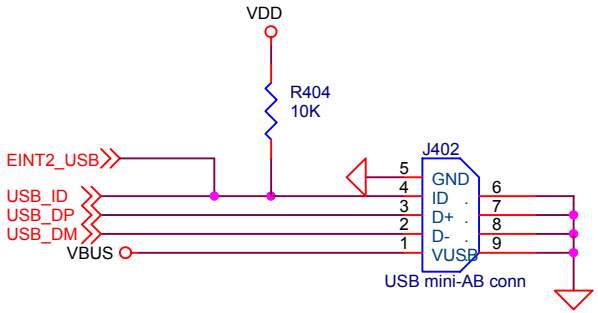
Schematics Design for USB2.0 OTG

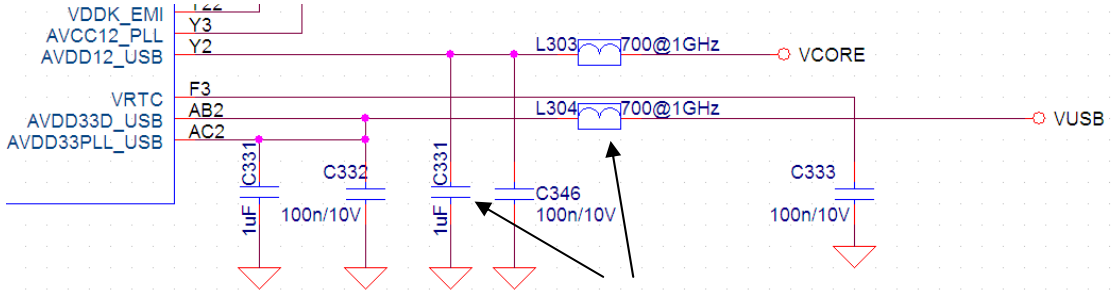
- Take MT6238 for example



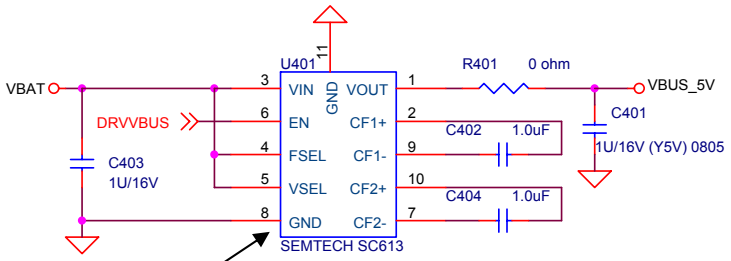


Must be 5.1K ohm, 1%
Place close to IC





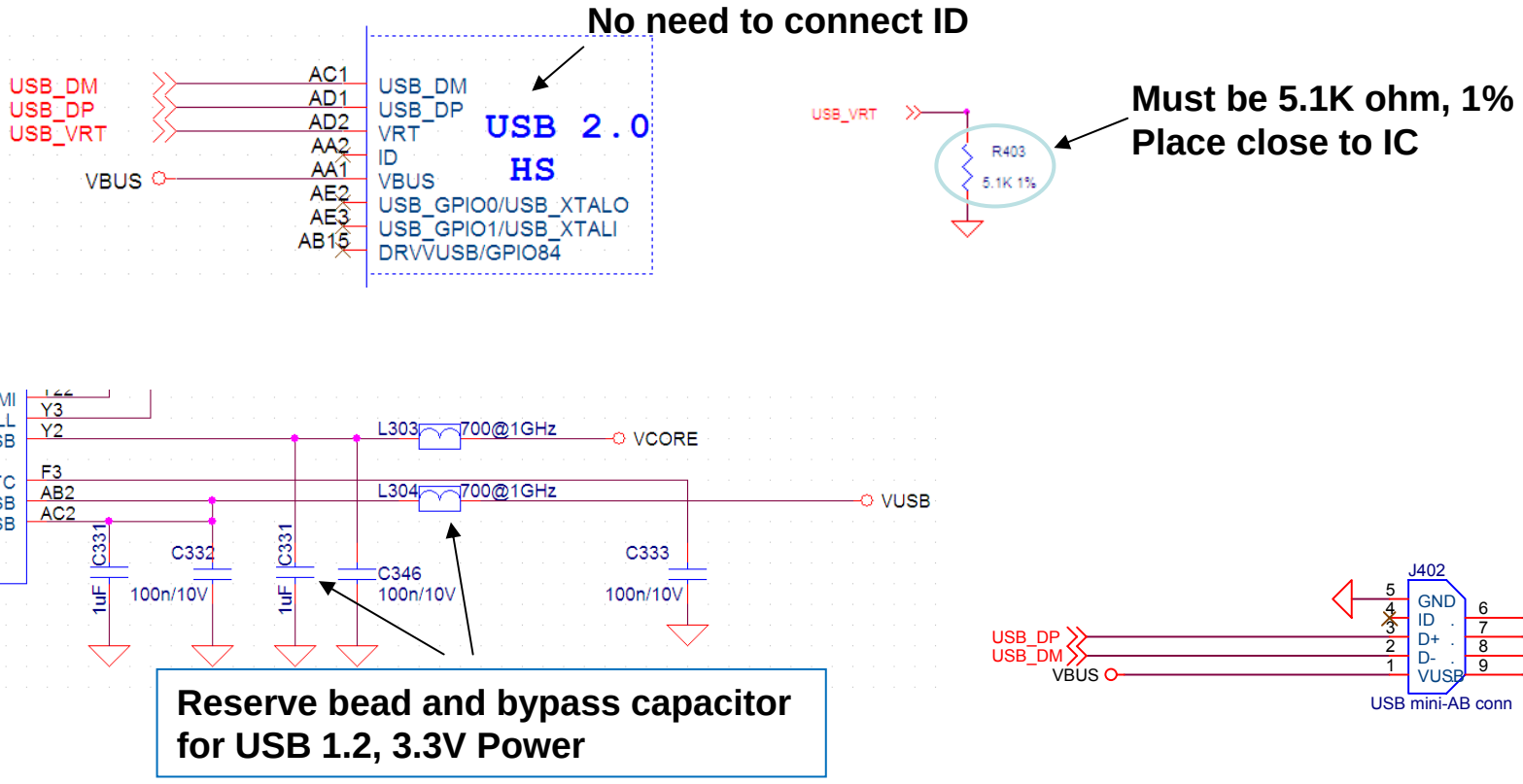
Reserve bead and bypass capacitor for USB 1.2, 3.3V power close to IC



Charge pump for OTG Power

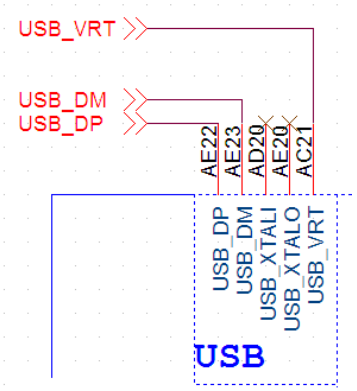
Schematics Design for USB2.0 Device (1/2)

- Take MT6238 for example

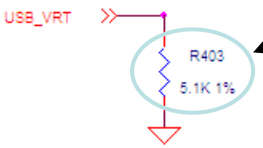


Schematics Design for USB2.0 Device (2/2)

- Take MT6235 for example

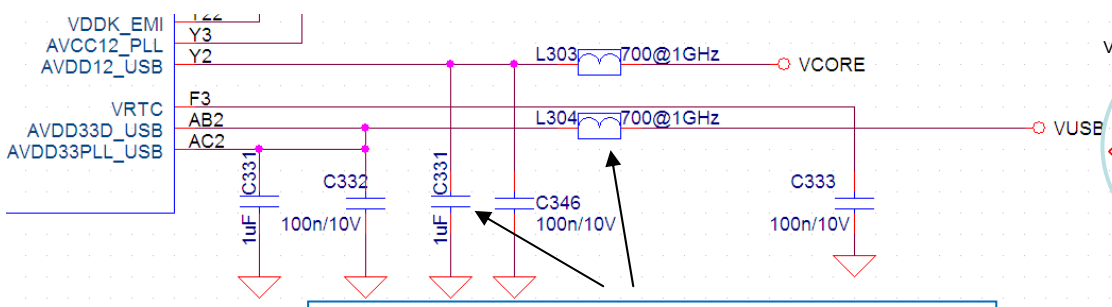


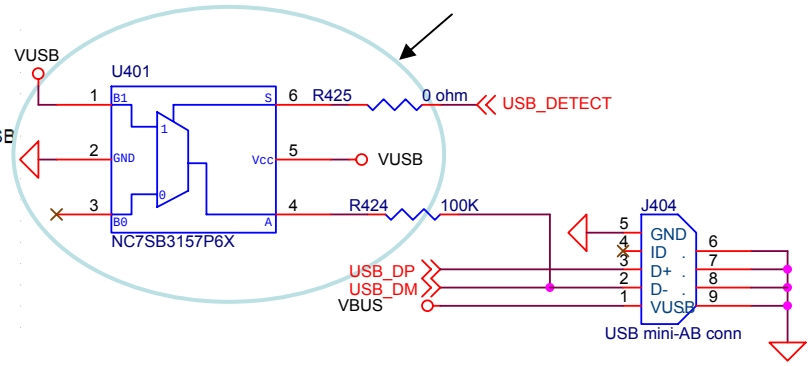
No VBUS, Different from MT6238



Must be 5.1K ohm, 1%
Place close to IC

For USB/ standard charger detection, Different from MT6238

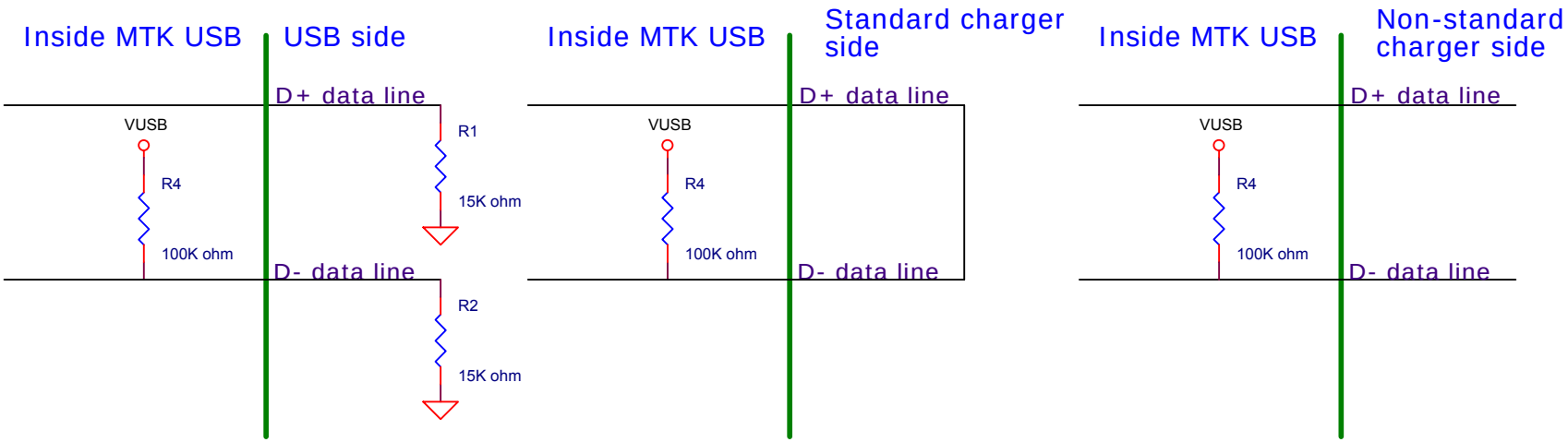




Reserve bead and bypass capacitor for USB 1.2, 3.3V Power

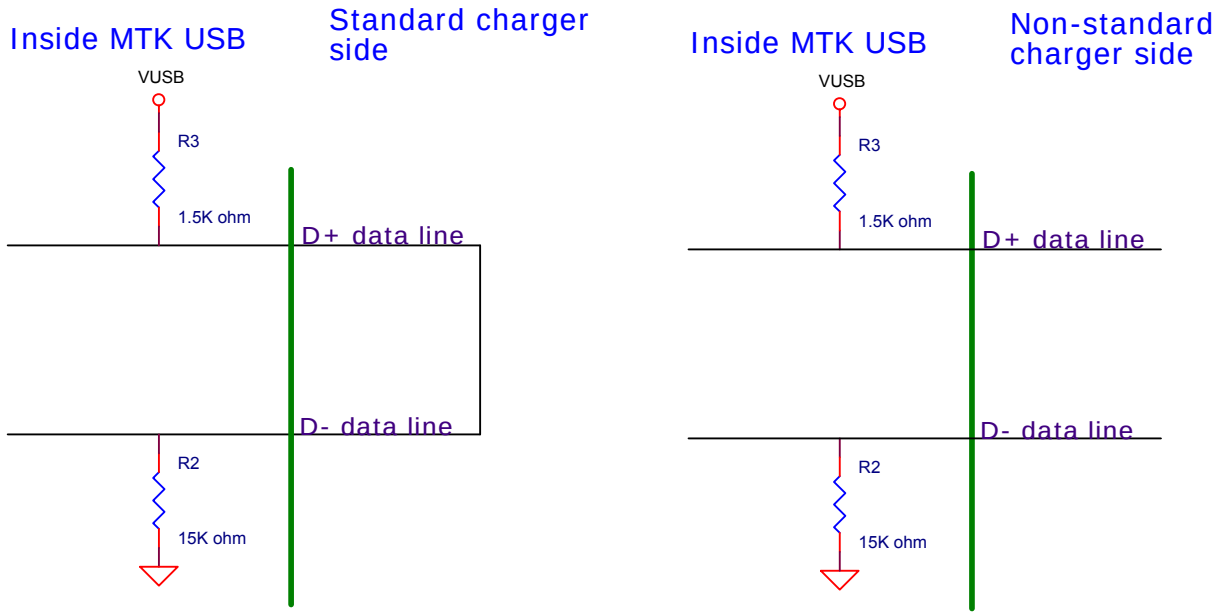
USB/ Charger Detection

- Used for MT6238 and later on MTK ICs
- When charger interrupt happens, turn on D- pull high 100K ohm resistor and check the polarity of D-
  - If the D- is HIGH, it is USB charger, otherwise it is a standard or a non-standard charger



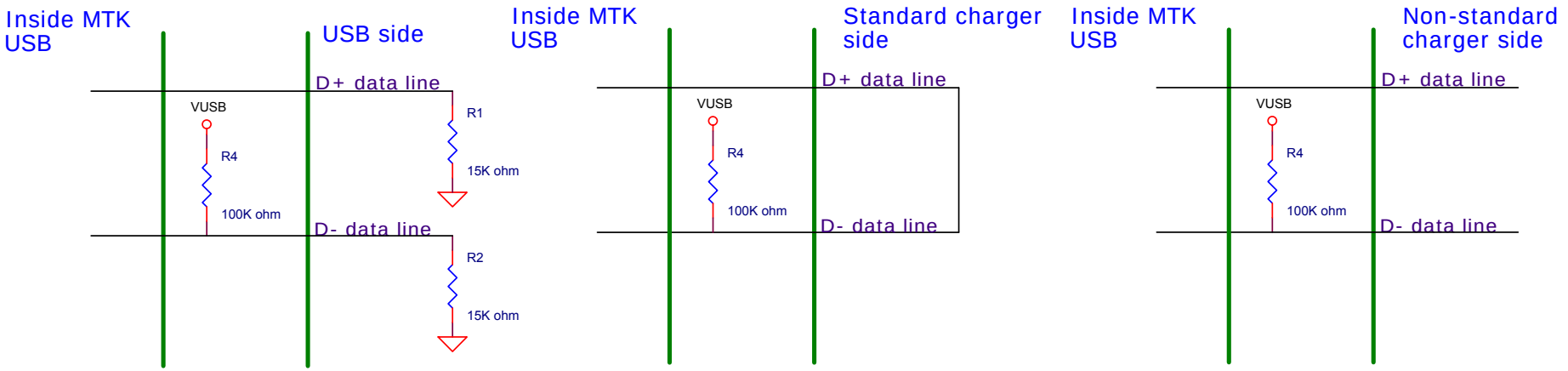
USB/ Charger Detection (Cont.)

- Then check whether it is standard or non-standard charger. Turn on D+/D- internally 15K ohm pull low resistor and D+ 1.5K ohm pull high resistor at the same time.
  - Check D- polarity. If the D- is HIGH, it is standard charger, otherwise it is a non-standard charger.



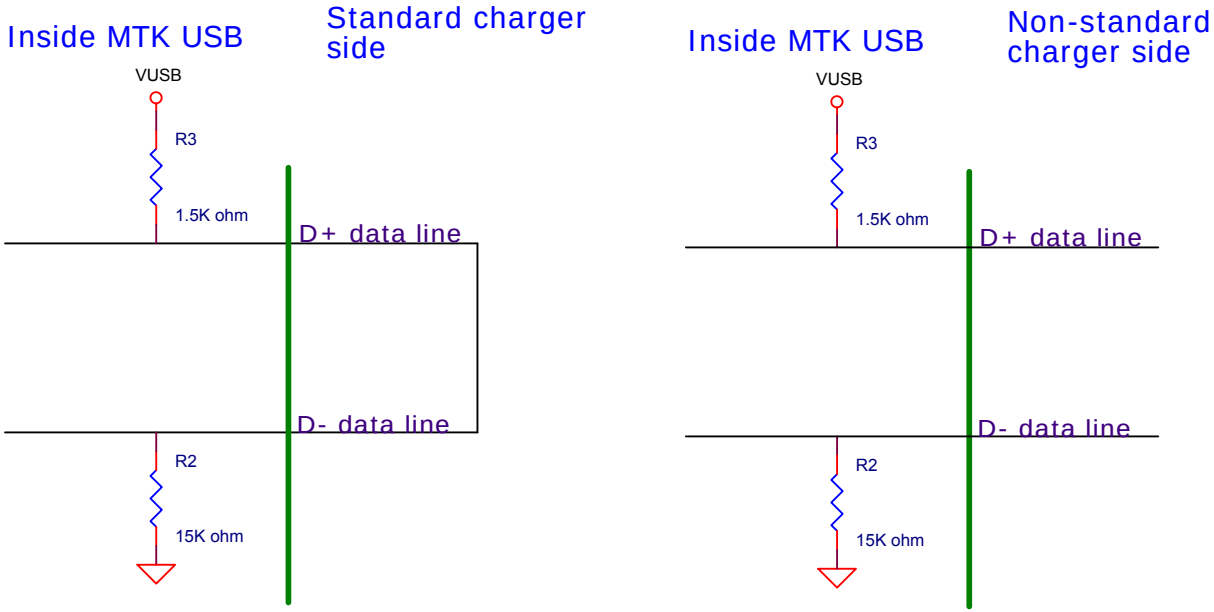
MT6235 USB/ Charger Detection Proposal

- For MT6235, R4 and analog switch are not integrated into IC.
- Same as MT6238, but use external 100K ohm pull high resistor
  - If the D- is HIGH, it is USB charger, otherwise it is a standard or a non-standard charger



MT6235 USB/ Charger Detection (Cont.)

- Then check whether it is standard or non-standard charger. Turn on D+/D- internally 15K ohm pull low resistor and D+ 1.5K ohm pull high resistor at the same time.
  - Check D- polarity. If the D- is HIGH, it is standard charger, otherwise it is a non-standard charger.



High Speed USB Layout Checklist (1/2)

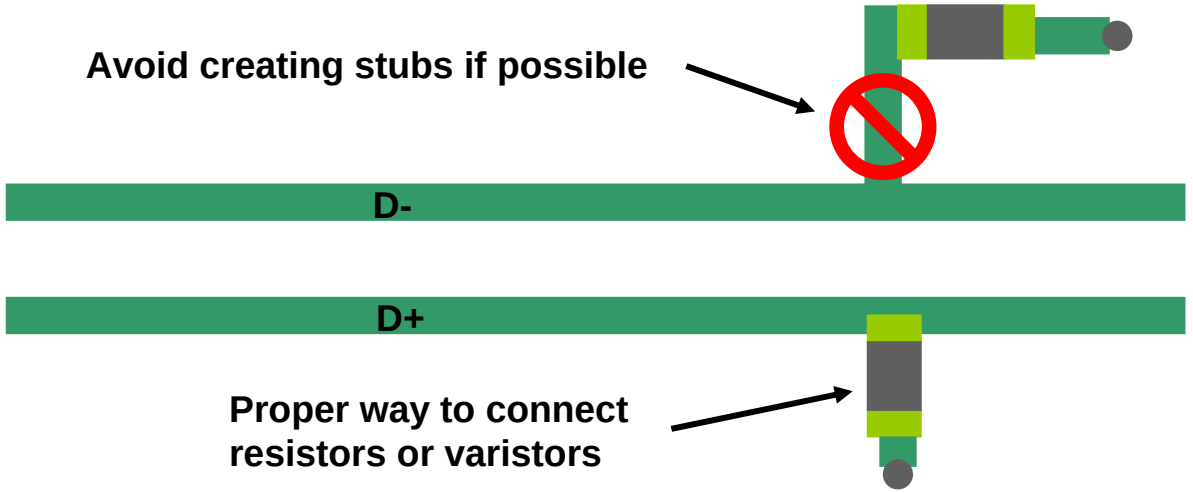
- General design and layout rules
  - With minimum trace lengths, route clock source and HS USB differential pairs first. Keep maximum possible distance between clocks/periodic signals to USB differential pairs to minimize crosstalk.
  - Route HS USB signal pairs together with equal length by using a minimum vias and corners. This reduces signal reflections and impedance changes.
  - Maintain parallelism between USB differential signals with the trace spacing needed to achieve 90 ohms differential impedance.
  - When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal by minimizing impedance discontinuities.
  - Do not route USB traces under crystals, oscillators, clock synthesizers, magnetic devices or ICs that use and/or duplicate clocks.

High Speed USB Layout Checklist (2/2)

- General design and layout rules (Conti.)
  - Stubs on HS USB signals should be avoided, as stubs will cause signal reflections and affect signal quality.
  - Avoid crossing over anti-etch if possible. Crossing over anti-etch (plane splits) increases inductance and radiation levels by forcing a greater loop area. Likewise, avoid changing layers with high-speed traces as much as practical.
  - Keep HS USB signals away from high current area. The current transient during state transitions could induce noise to USB.

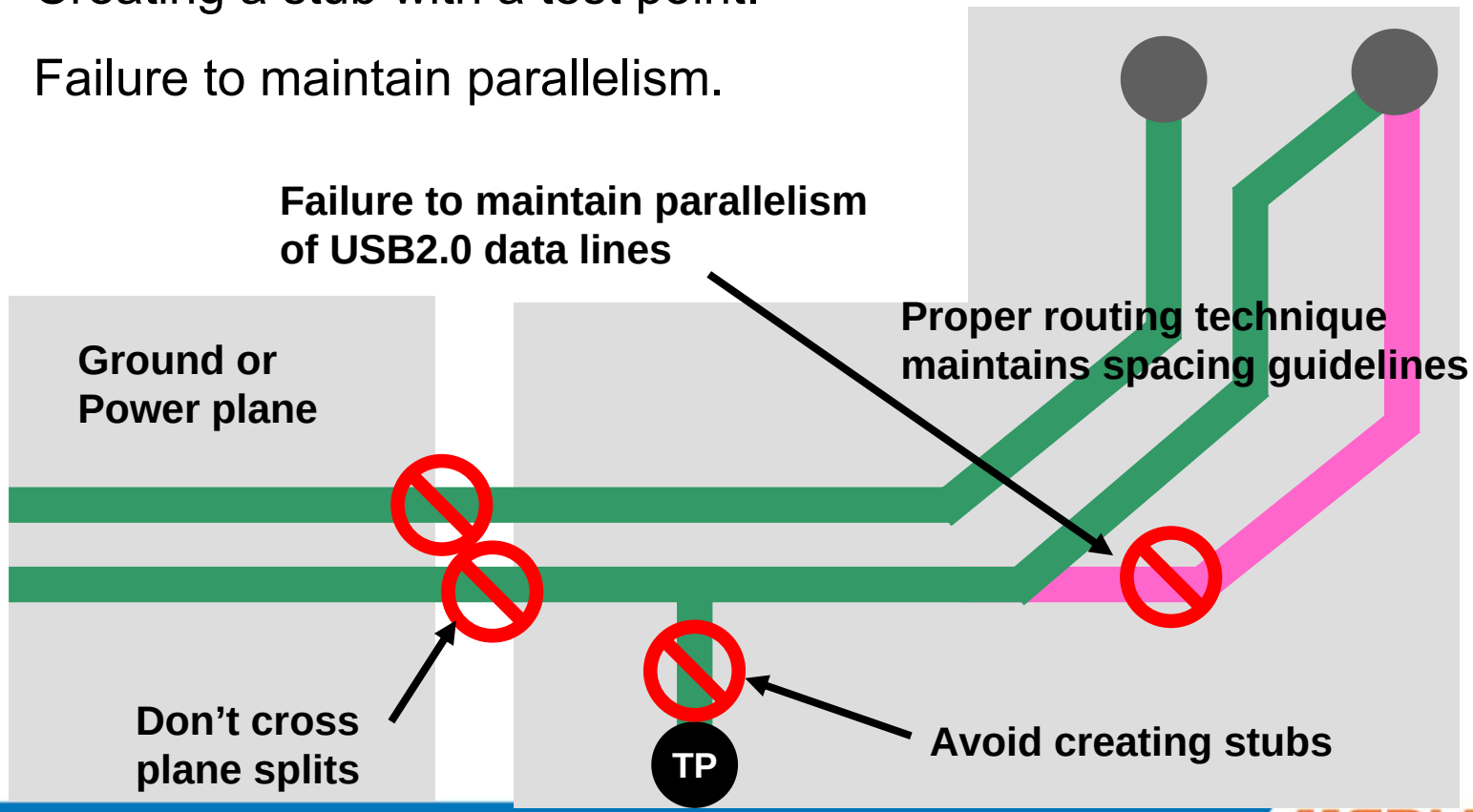
Stubs

- Avoid creating unnecessary stubs on data lines, if a stub is unavoidable (for example: ESD issue), please keep the stub as short as possible.



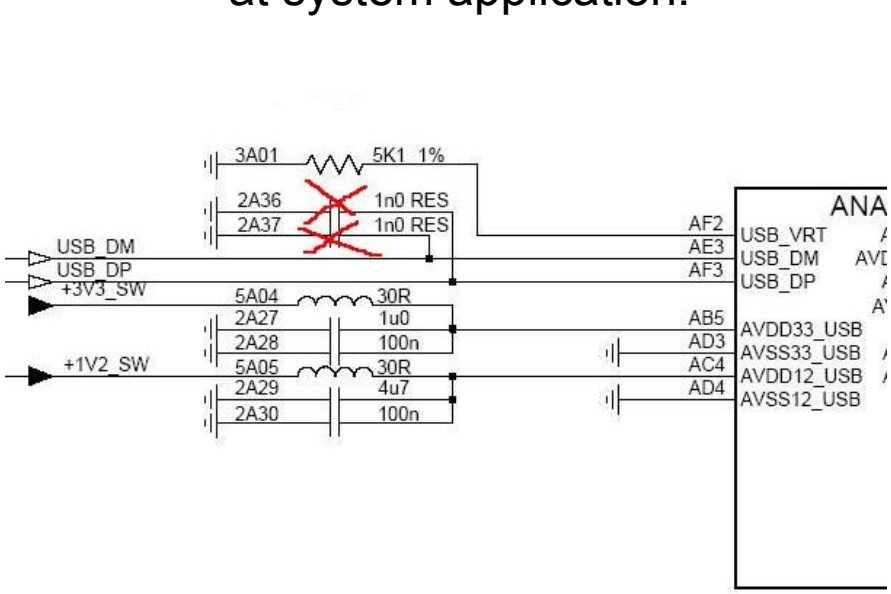
Poor Routing Techniques

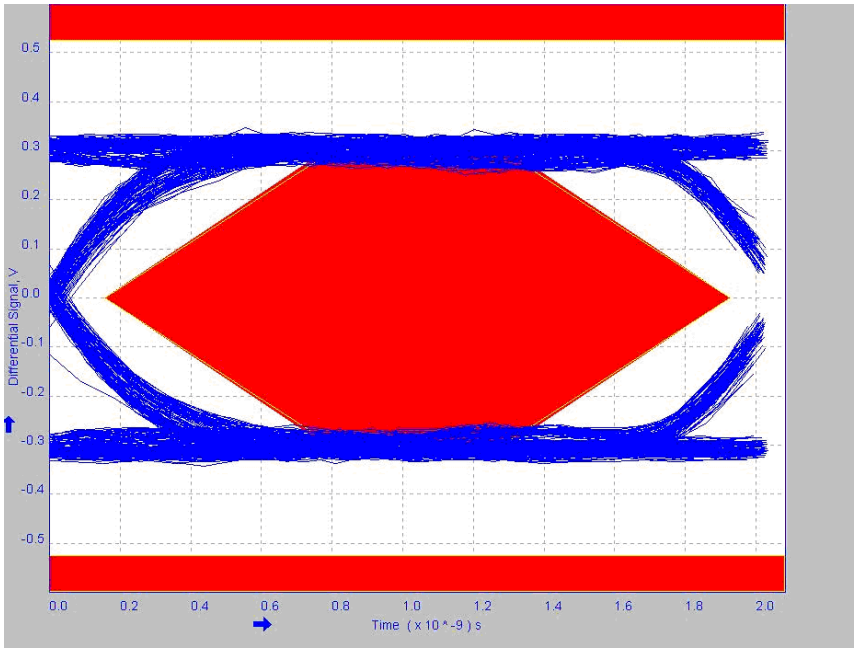
- Cross a plane split.
- Creating a stub with a test point.
- Failure to maintain parallelism.



Case Study (1/5)

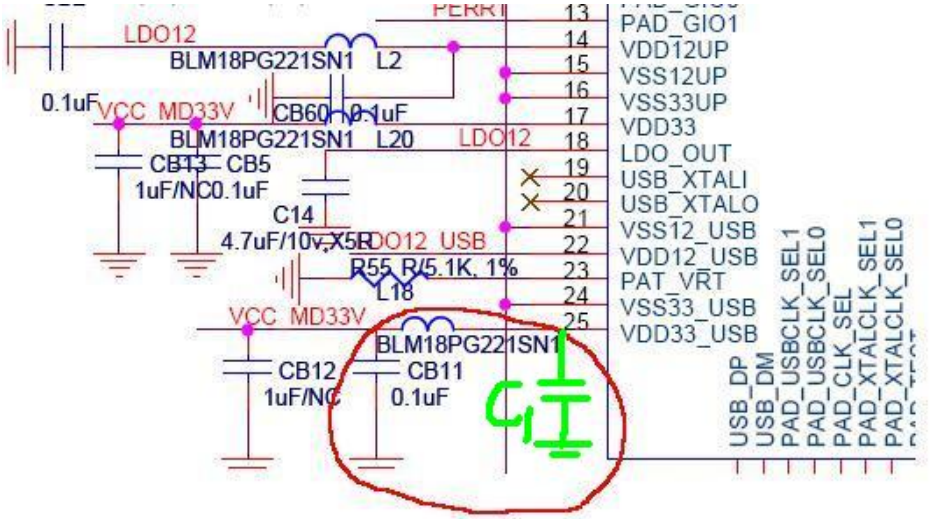
- Case 1:
  - 2A36/2A37 should be removed. Large cap at USB_DP/USB_DM will lead to bad jitter performance.
  - Measured eye at board is shown below. It will occur turn-around error at system application.

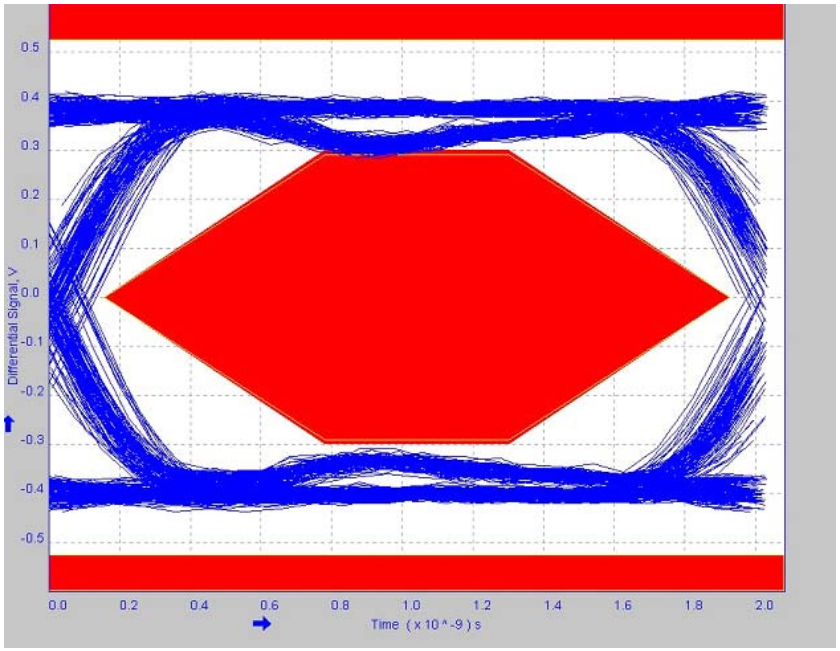




Case Study (2/5)

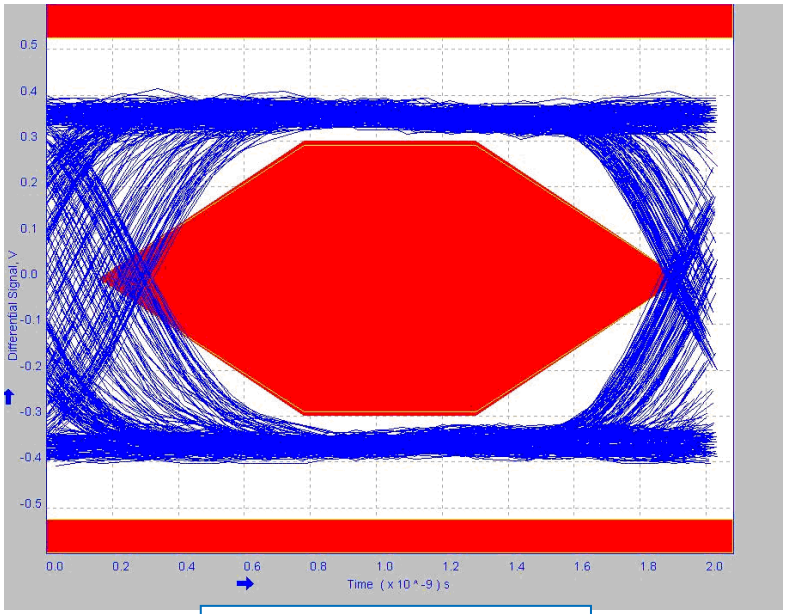
- Case 2:
  - After bead, at least 0.1uF capacitor between VDD33_USB, VDD12_USB and ground must be added as follows.
  - Measured eye diagram has bad jitter performance.



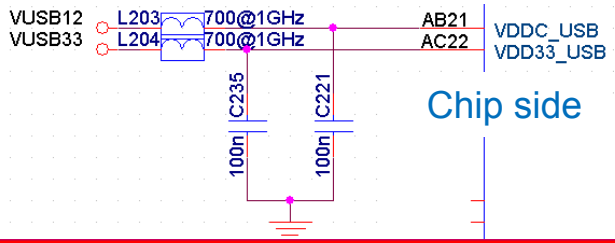


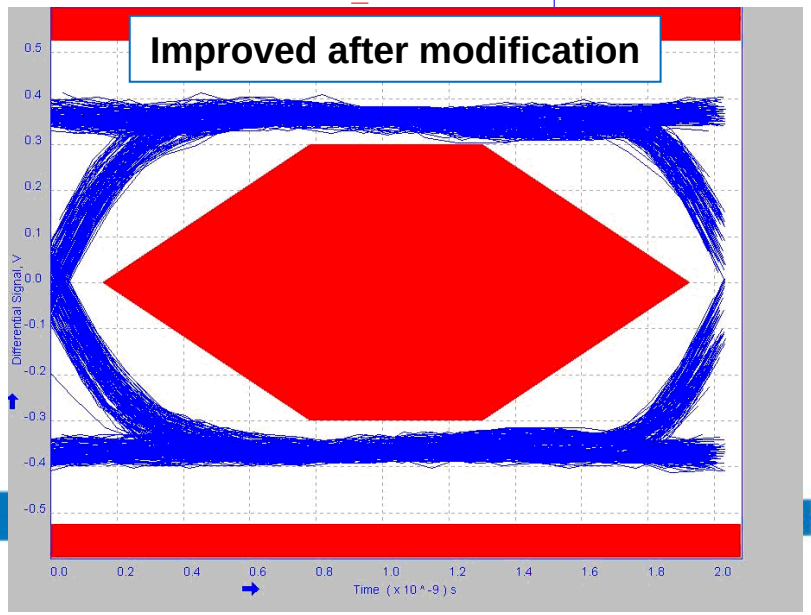
Case Study (3/5)

- Case 3:
  - Some time we got worse jitter due to poor layout, then VUSB33 and VUSB12 are coupled by noise.
  - It is improved by increasing bypass capacitor C221 and C235.



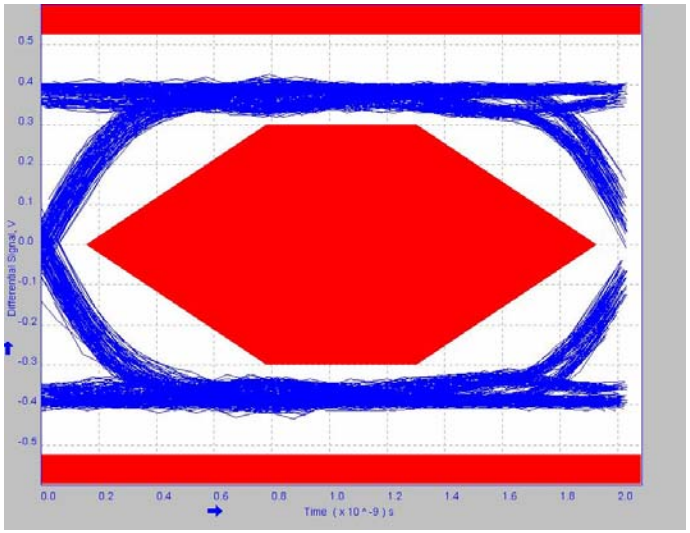
Before modification



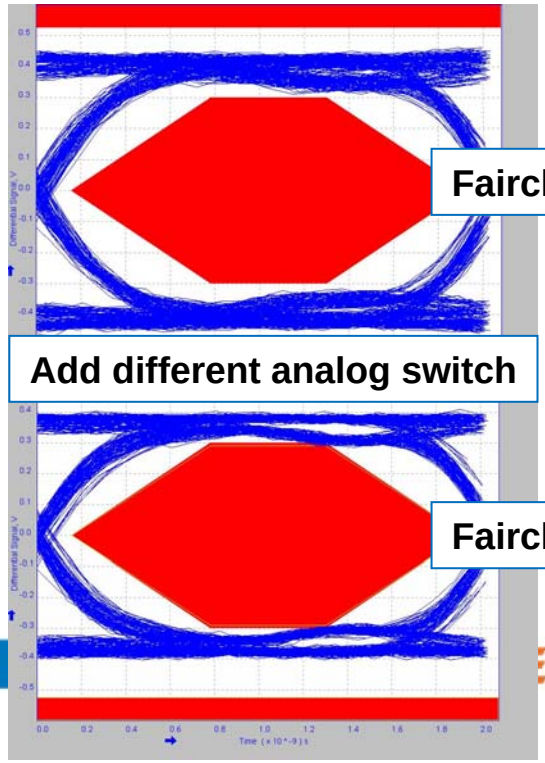


Case Study (4/5)

- Case 4:
  - Customer wants to share USB data pins with audio/UART pins through the same 5-wire USB connector by using analog switch.
  - Different analog switches cause different attenuation of signals; please make sure component and layout will get proper eye diagram.
  - No suggestion on using analog switch, 11-pin USB connector could be used instead.



Original design without analog switch



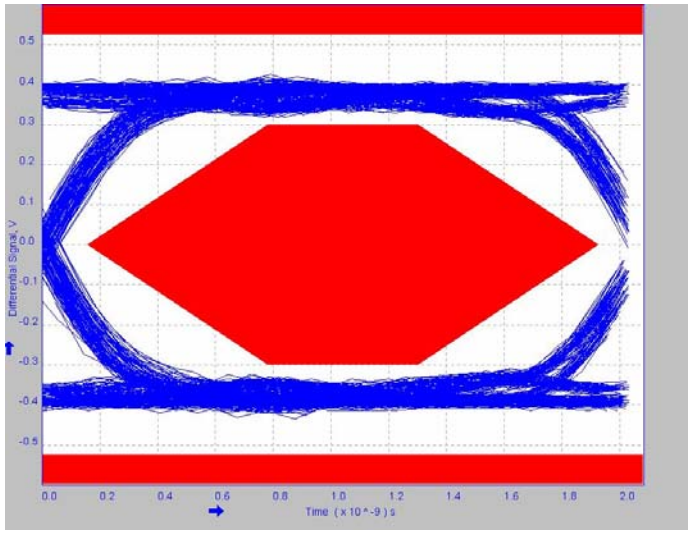
Fairchild FSUSB42

Add different analog switch

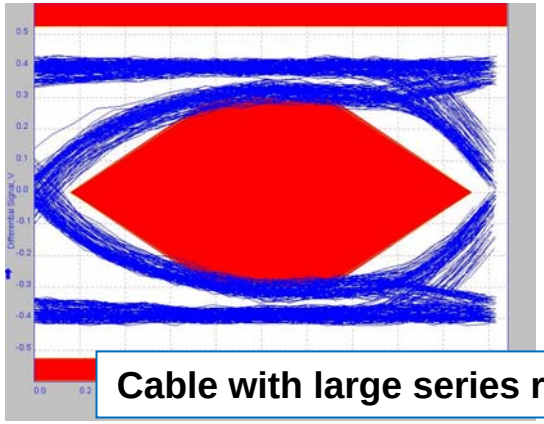
Fairchild FSUSB30

Case Study (5/5)

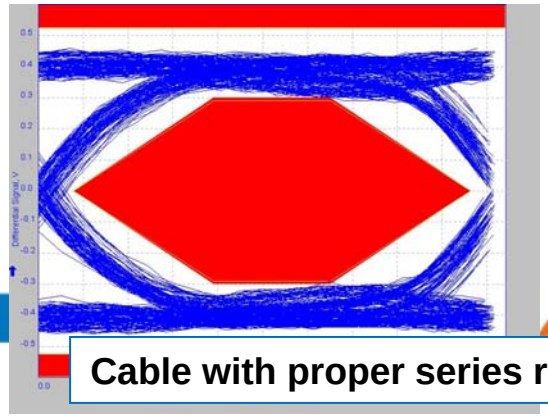
- Case 5:
  - Sometimes customer may design a special connector for USB, such as 18-pin I/O.
  - Poor cable will cause poor performance.
  - Please follow USB cable design guide.



Design with normal USB cable



Cable with large series resistance



Cable with proper series resistance

USB/ OTG Cable Design

High Speed USB Cable Design

- Besides PCB layout, the cable design affects USB 2.0 performance much.
- If using standard USB HS/FS cables for front panel support ensure they meet all cabling requirements called out in Chapter 6 of the USB 2.0 Specification .
- If custom cables are used, verify the requirements of USB 2.0 cable specification of the design guideline are followed.

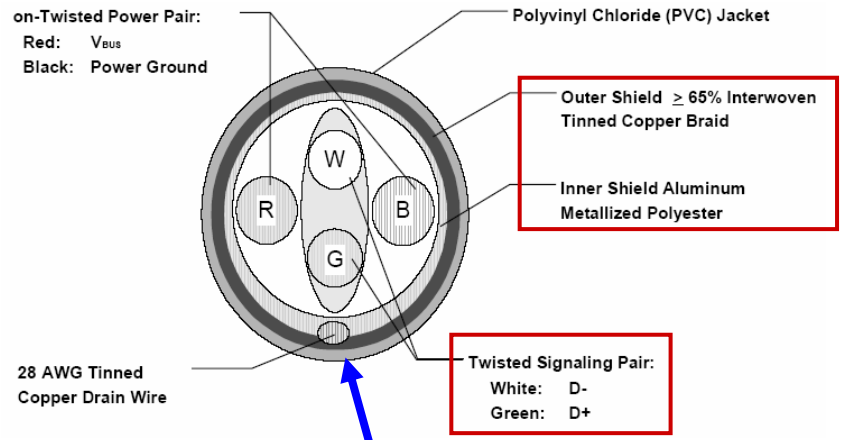
USB Cable Design Concept

- There are two type of cables need to be designed for the purpose of passing the specification of USB2.0 OTG
  - One is used for connecting to PC, normally mobile phone acts as a slave.
  - The other is used for connecting to external devices such as mass storage devices, normally mobile phone acts as a host.

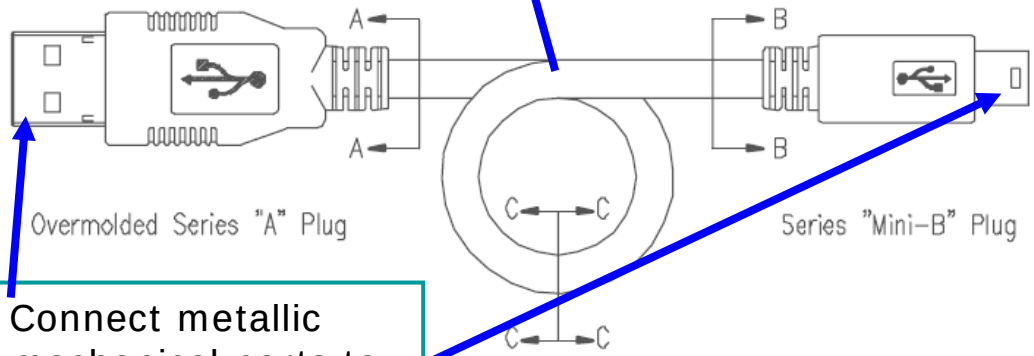
- Each cable design is based on the specification defined in
  - “Universal Serial Bus Specification” Revision 2.0, April 27, 2000
  - “USB 2.0 Specification Engineering Change Notice # 1: Mini-B connector”, 10/20/2000
  - “On-The-Go Supplement to the USB 2.0 Specification” Revision 1.0a, June 24, 2003

General USB Cable for USB2.0 (Mobile as Slave)

- Enhance grounding to minimize clock skew

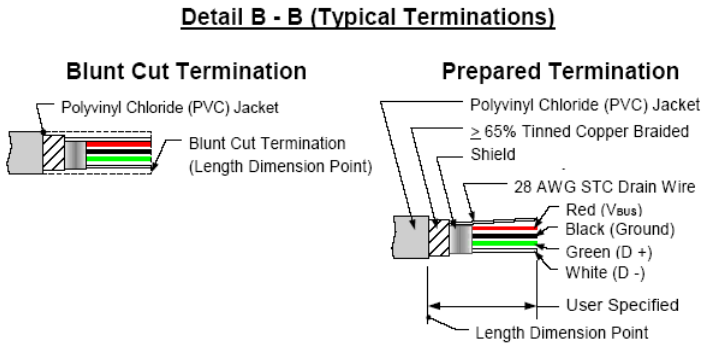


C-C Cross-section View



Connect metallic mechanical parts to Ground Signal.

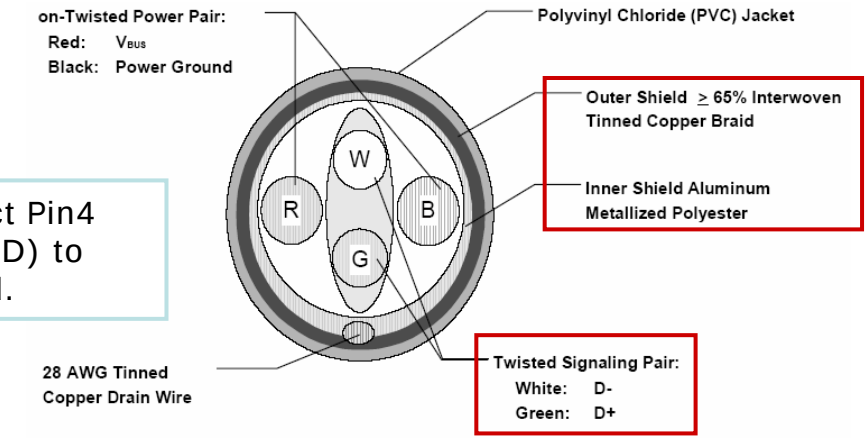
The DC resistance from plug to plug must be less than 0.6 ohms.



General A to mini-B USB 2.0 cable

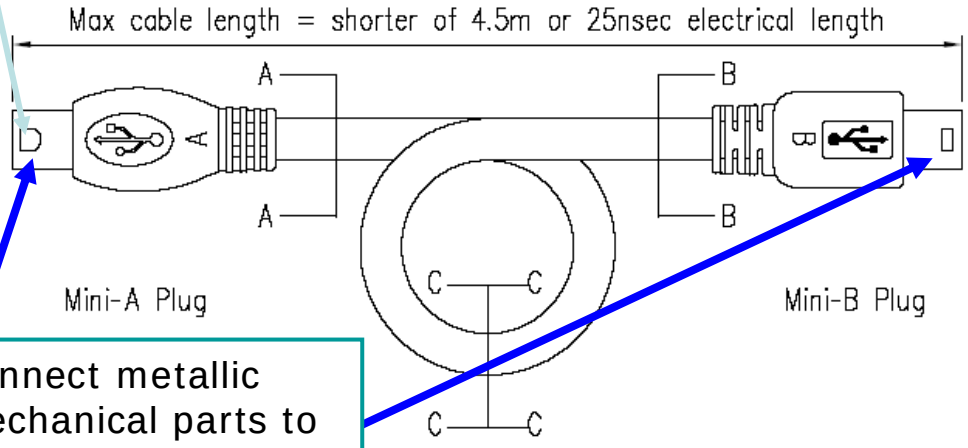
General USB Cable for USB2.0 (Mobile as Host)

- Enhance grounding to minimize clock skew



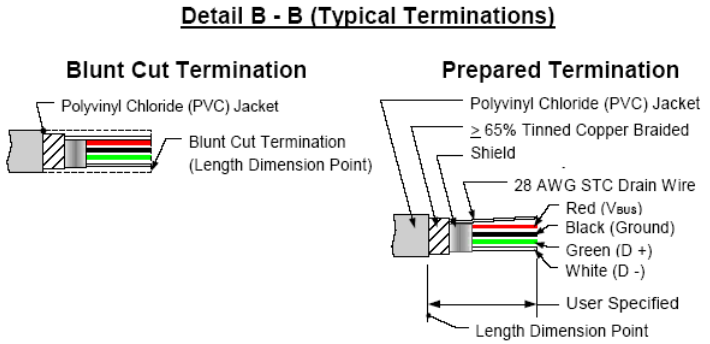
C-C Cross-section View

Connect Pin4 (USB_ID) to Ground.



Connect metallic mechanical parts to Ground Signal.

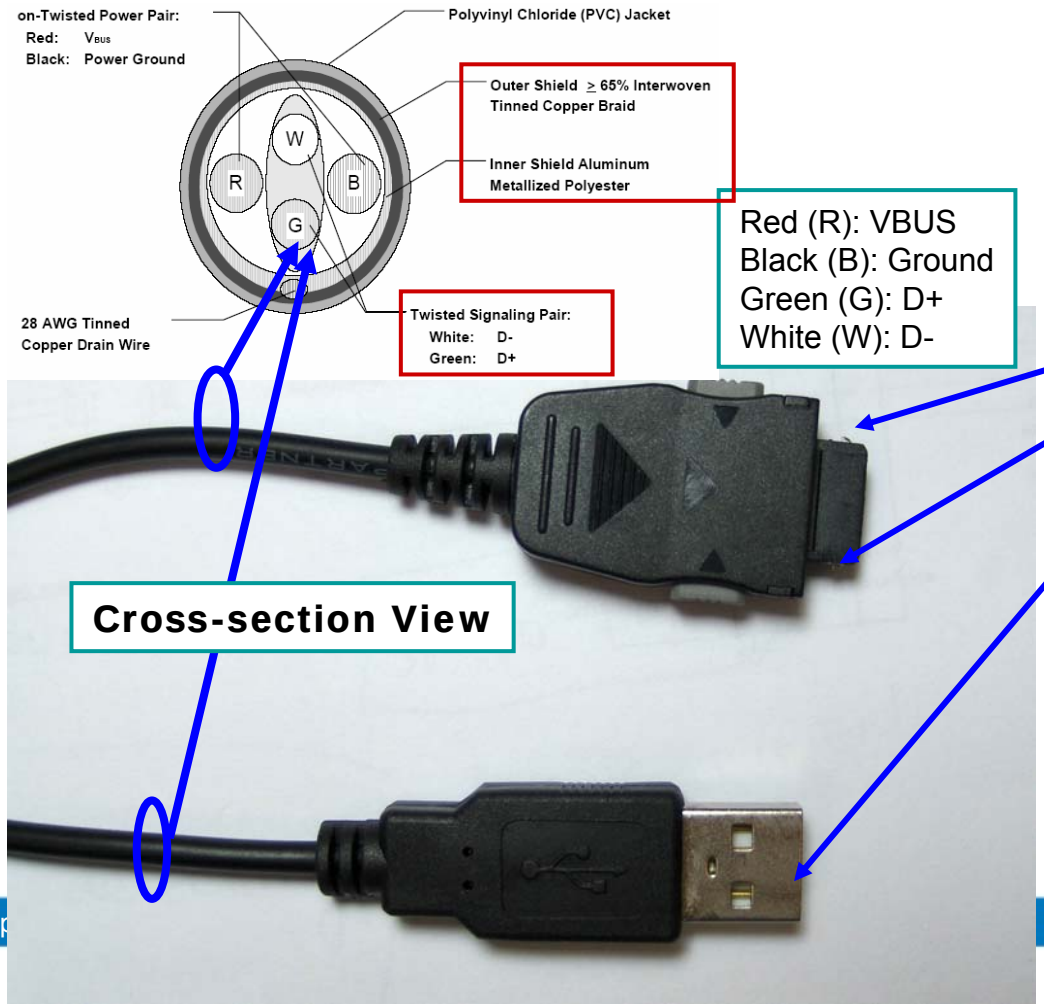
The DC resistance from plug to plug must be less than 0.6 ohms.



Mini-A to mini-B USB 2.0 cable

18-pin USB Cable for USB2.0 (Mobile as Slave)

- Enhance grounding to minimize clock skew



The DC resistance from plug to plug must be less than 0.6 ohms.

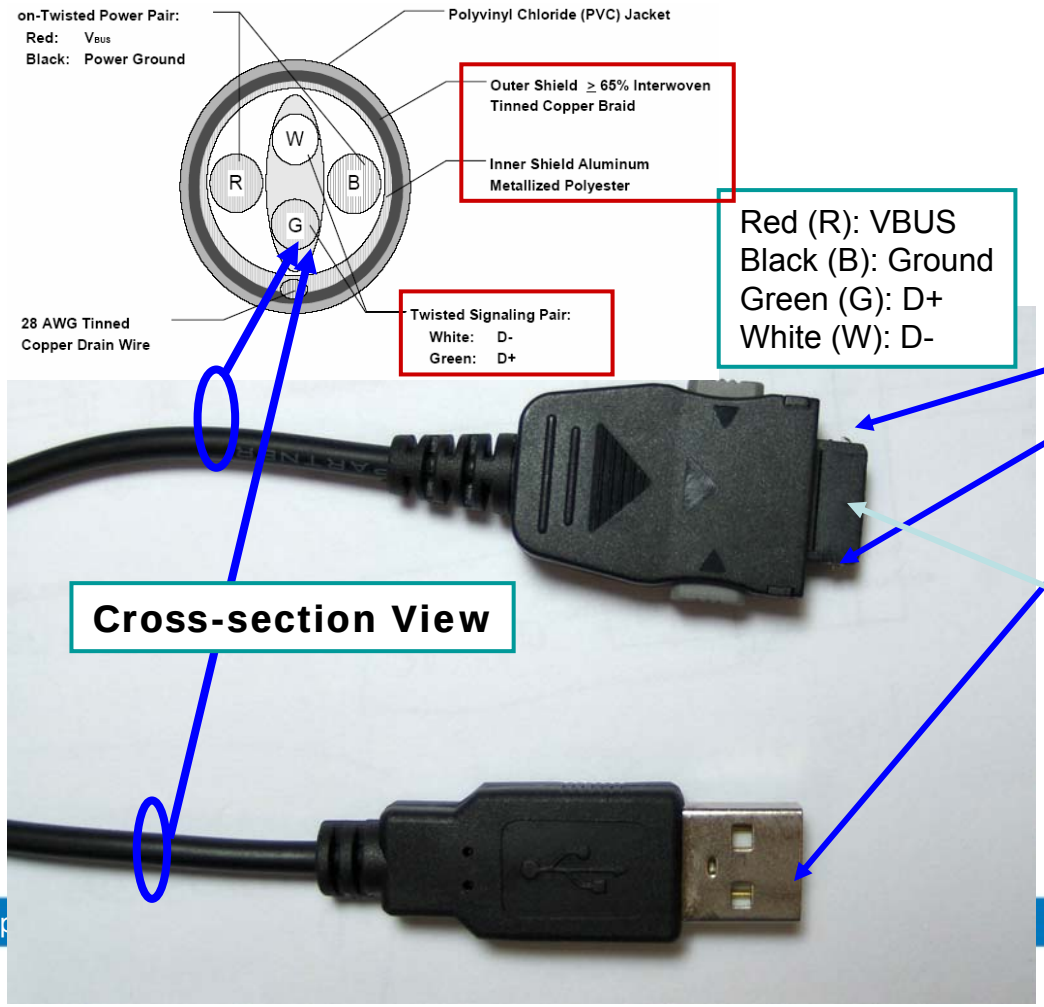
Red (R): VBUS
Black (B): Ground
Green (G): D+
White (W): D-

Connect metallic mechanical parts to Ground Signal.

18pin connector to type-A connector

18-pin USB Cable for USB2.0 (Mobile as Host)

- Enhance grounding to minimize clock skew



The DC resistance from plug to plug must be less than 0.6 ohms.

Red (R): VBUS
Black (B): Ground
Green (G): D+
White (W): D-

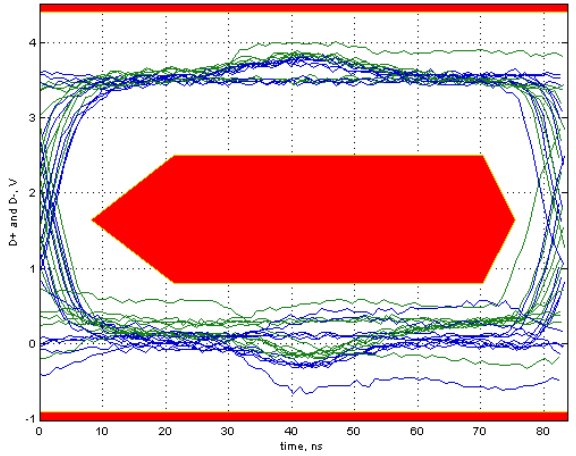
Connect metallic mechanical parts to Ground Signal.

Connect USB_ID pin to Ground.

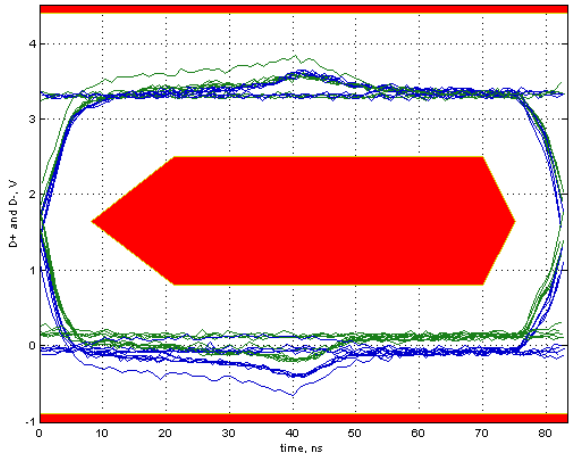
18pin connector to type-A connector

Why Emphasize on Grounding (full speed)

- One of customer's phone design uses 18-pin connector as USB I/O, and there is only one ground pin.
  - USB performance is poor even it's full speed USB
  - Jitter large
  - Eye diagram marginally pass

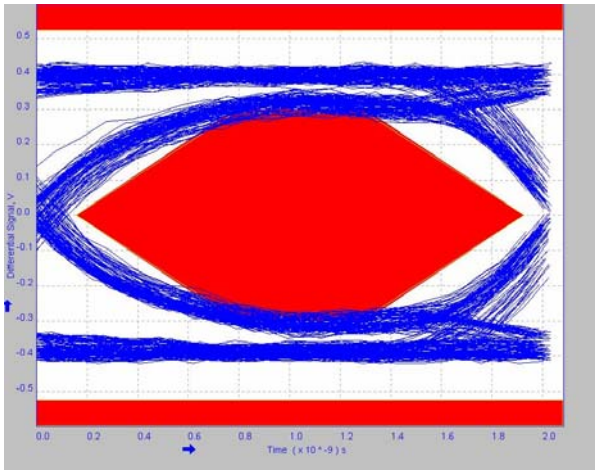


- Enhance grounding as shown in last page
  - Pass the USB-IF certification

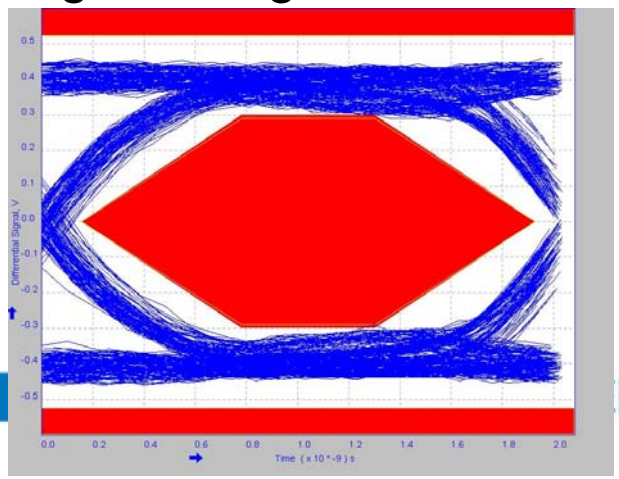


Why Emphasize on Grounding (high speed)

- Uses 18-pin connector as USB I/O, with two ground pins and no shielding on data pins
  - USB performance is poor
  - Jitter large
  - Eye diagram fail
  - Rise time longer



- Modified cable with enhanced shielding and grounding, minimize series resistor.
  - Pass the USB-IF certification



Conclusion

- Layout and component selection are critical for USB2.0 high speed performance
  - Need to follow the design rule or there might be compatibility issue happens

- Grounding and shielding are both critical when design USB2.0 high speed capable cables
  - It can maintain USB signal quality with little jitter/ signal distortion caused by cable design

Reference

- USB-IF “Universal Serial Bus Specification” Revision 2.0, April 27, 2000
- USB-IF “USB 2.0 Specification Engineering Change Notice # 1: Mini-B connector”, 10/20/2000
- USB-IF “On-The-Go Supplement to the USB 2.0 Specification” Revision 1.0a, June 24, 2003
- Intel “High Speed USB Platform Design Guidelines” Revision 1.0, 07/12/2000

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