# **Bluetooth Module Datasheet**

CZW-3031-03

Model:CZW-3031-03

Hardware Version: V2.0

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Shenzhen

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### 1 summary

CZW-3031-03 is a Bluetooth module designed by ShenZhen Cheng Zhi Wei Technology Co.,Ltd. using Qualcomm Bluetooth chip qcc3031。

CZW-3031-03 is a Bluetooth, audio and programmable application processor. It includes high-performance, analog, and digital audio codecs, Class-AB speaker driver, advanced power management, Li-ion battery charger, light-emitting diode (LED) drivers, and flexible interfaces including inter₁ integrated circuit sound (I²S), inter-integrated circuit interface (I²C), universal asynchronous receiver transmitter (UART), and programmable input/output (PIO).

CZW-3031-03 package is compatible with czw03 series pins, easy replacement and upgrade

## 2 General specifications

Model Name	CZW-3031-03
Package	60 Pin Module
Dimension	13.8mm x 20.5mm x 2.4mm
Chipset	QCC3031
Bluetooth Version	Bluetooth 5.0
Power Class	Class2
Transmission Distance	≥10M
Voltage	2.8~4.2V
Temperature	-10∼+70℃
Storage Temperature	-40∼+85℃
Frequency Range	2402~2480MHz
Maximum RF Transmit Power	9dBm
π/4 DQPSK Receive Sensitivity	-91dBm
8DPSK Receive Sensitivity	-81dBm

### 3 Key Features

### 3.1 Device description

- ★ High-performance programmable Bluetooth® stereo audio SoC with Qualcomm® aptX™ audio
- ★ Fully qualified single-chip dual-mode Bluetooth v5.0 system
- ★ Tri-core processor architecture with low power for extended battery life

#### 3.2 Features

- ★ Qualified to Bluetooth® v5.0 specification
- ★ 120 MHz Qualcomm® Kalimba™ audio DSP
- ★ 32 MHz Developer Processor for applications
- ★ Firmware Processor for system
- ★ Flexible QSPI flash programmable platform
- ★ Advanced audio algorithms
- ★ High-performance 24- bit stereo audio interface
- ★ Digital and analog microphone interfaces
- ★ Flexible PIO controller and LED pins with PWM support
- ★ 1-mic Qualcomm® cVc<sup>™</sup> speaker noise reduction and echo cancellation technology
- ★ aptX, aptX HD, aptX Low Latency, SBC, and AAC audio codecs support
- ★ Serial interfaces: UART, Bit Serializer (I<sup>2</sup> C/SPI), USB 2.0
- ★ Integrated PMU: Dual SMPS for system/digital circuits, Integrated Li-ion battery charger

### 3.3 Audio subsystem

- ★ 32 bit Kalimba audio digital signal processor (DSP) core with flexible clocking from 2 MHz to 120 MHz to allow optimization and trade-off performance vs. power consumption
- ★ DSP runs from ROM
- ★ 80 KB program random access memory (RAM)
- ★ 256 KB data RAM
- ★ 5 Mb ROM

### 3.4 Application subsystem

- ★ Dual core application subsystem 32 MHz operation
- ★ 32 bit Firmware Processor:
- ★ 32 bit Developer Processor:
- ★ Both cores execute code from external flash memory using QSPI clocked at 32 MHz
- ★ On-chip caches per core allow for optimized performance and power consumption

### 3.5 Bluetooth subsystem

- ★ Qualified to Bluetooth v5.0 specification including 2 Mbps Bluetooth low energy (Production parts)
- ★ Single ended antenna connection with on-chip balun and Tx/Rx switch
- ★ Bluetooth, Bluetooth low energy, and mixed topologies supported
- ★ Class 1 support

#### 3.6 Li-ion battery charger

- ★ Integrated battery charger supporting internal mode (up to 200 mA) and external mode (up to 1.8 A)
- ★ Variable float (or termination) voltage adjustable in 50 mV steps from 3.65 V to 4.4 V
- ★ Thermal monitoring and management are implementable in application software
- ★ Pre-charge to fast charge transition configurable at 2.5 V, 2.9 V, 3.0 V, and 3.1 V

### 3.7 Power management

- ★ Integrated power management unit (PMU) to minimize external components
- ★ runs directly from a Li-ion, USB, or external supply (2.8 V to 6.5 V)
- ★ Auto-switching between battery and USB (or other) charging source
- ★ Power islands employed to optimize power consumption for variety of use-cases
- ★ Dual switch-mode power supply (SMPS)

### 3.8 Audio engine and digital audio interfaces

- ★ 24-bit I<sup>2</sup> S interface with 1 input and 3 output channels
- ★ Programmable audio master clock (MCLK)
- ★ Sony/Philips digital interface (SPDIF): 2, configurable as input or output
- ★ Stereo analog Class-AB headphone outputs:
- ★ Dual analog inputs configurable as single ended line inputs or, unbalanced or balanced analog microphone inputs
- ★ 1 microphone bias (single bias shared by the two (channels)
- ★ Digital microphone inputs with capability to interface up to 6 digital microphones
- ★ Both analog-to-digital converter (ADC)s and digital-to<sub>1</sub> analog converter (DAC)s support sample rates of 8, 16, 32, 44.1, 48, 96 kHz. DACs also support 192 kHz.

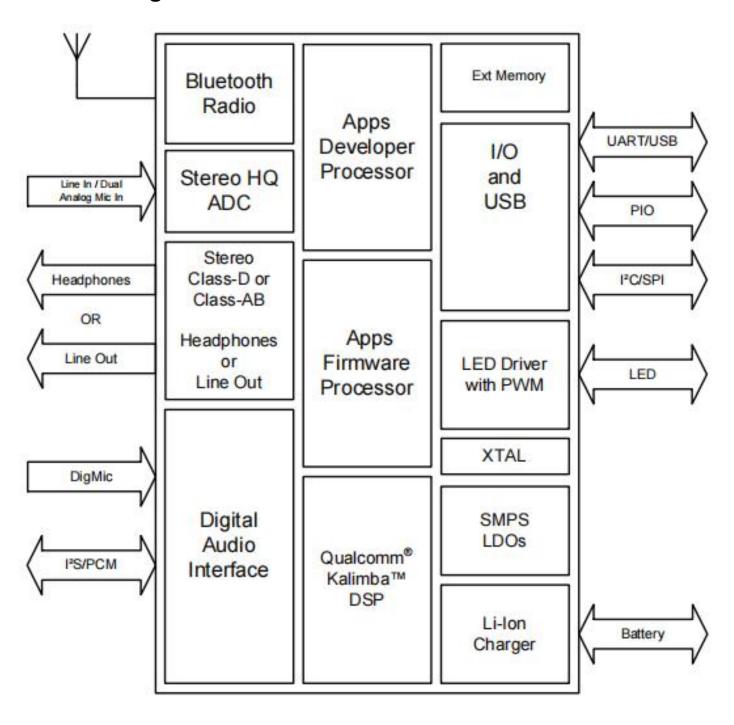
### 3.9 Peripherals and physical interfaces

- ★ A UART interface
- ★ 2 x Bit Serializers (programmable serial peripheral interface (SPI) and I<sup>2</sup> C hardware accelerator)
- ★ 1 x USB interface
- ★ QSPI NOR flash interface
- ★ Up to 17 PIO and 4 open drain/digital input LED pads with pulse width modulation (PWM)

# **4 Applications**

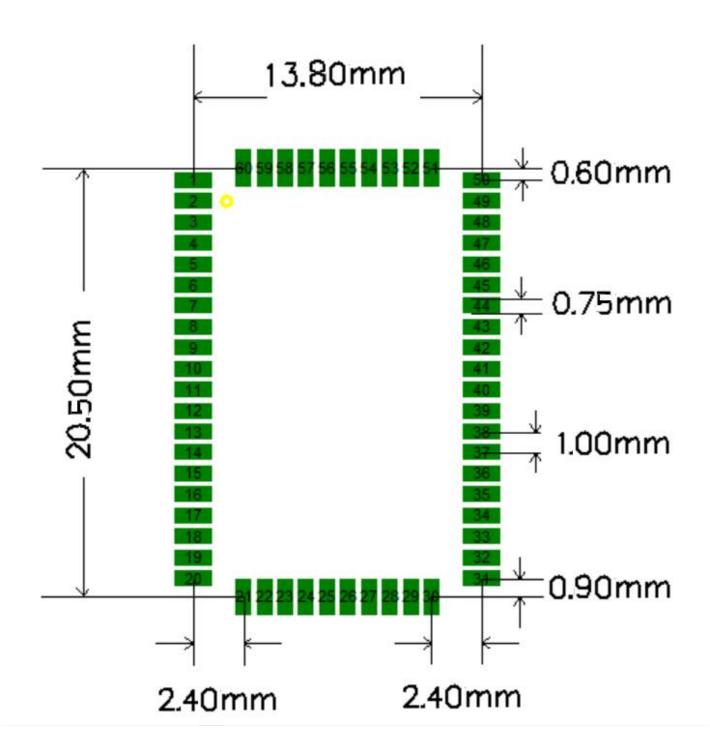
★ Wireless speakers

## **5 Block Diagram**

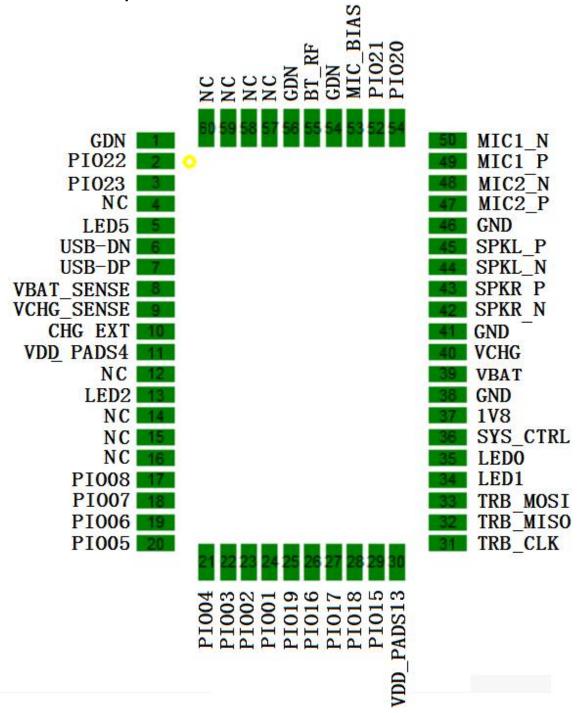


# **6 Module Package Information**

### 6.1 Pinout Diagram and package dimensions



#### **6.2 Module Pin descriptions**



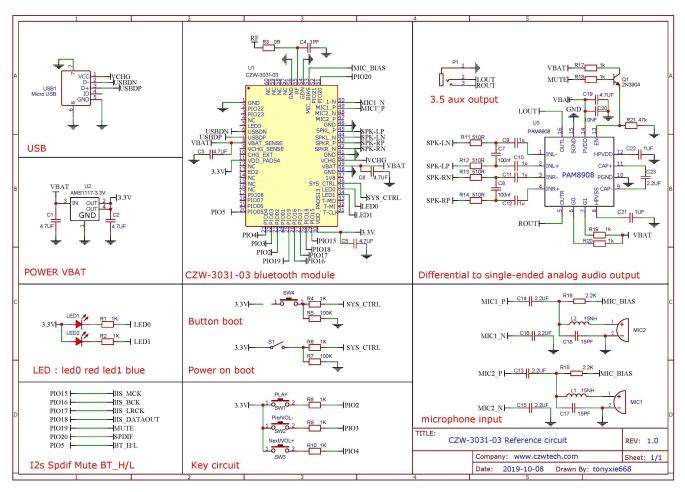
# **7 Pin Function Description**

Pin#	Pin Name	Pin type	Description
1	GND	Ground	Ground
2	PIO[22]	Digital: Bidirectional with programmable strength internal pull₁up/pull-down	Programmable I/O line 22.
3	PIO[23]	Digital: Bidirectional with programmable strength internal pull up/pull-down	Programmable I/O line 23.
4	NC	NC	NC
5	LED[5]	Analog or digital input/ open drain output.	General-purpose analog/digital input or open drain LED output.
6	USB_DN	Digital	USB Full Speed device D- I/O. IEC-61000-4-2 (device level) ESD Protection
7	USB_DP	Digital	USB Full Speed device D+ I/O. IEC-61000-4-2 (device level) ESD Protection
8	VBAT_SENSE	Analog	Battery voltage sense input.
9	VCHG_SENSE	Analog	Charger input sense pin after external mode sense-resistor. High impedance. NOTE If using internal charger or no charger, connect VCHG_SENSE direct to VCHG.
10	CHG_EXT	Analog	External charger transistor current control.  Connect to base of external charger transistor as per application schematic.
11	VDD_PADS_4	Supply	1.8 V/3.3 V PIO supply.
12	NC	NC	NC
13	LED[2]	Analog or digital input/ open drain output.	General-purpose analog/digital input or open drain LED output.
14	NC	NC	NC
15	NC	NC	NC
16	NC	NC	NC
17	PIO[8]	Digital: Bidirectional with programmable strength internal pull- up/pull-down	Programmable I/O line 8. Alternative function: TBR_CLK
18	PIO[7]	Digital: Bidirectional with programmable strength internal pull- up/pull-down	Programmable I/O line 7.  Alternative function: TBR_MISO[0]
19	PIO[6]	Digital: Bidirectional with programmable strength internal pull- up/pull-down	Programmable I/O line 6. Alternative function: TBR_MOSI[0]
20	PIO[5]	Digital: Bidirectional with programmable strength internal pull- up/pull-down	Programmable I/O line 5. Alternative function: TBR_MISO[1]
21	PIO[4]	Digital: Bidirectional with programmable strength internal pull- up/pull-down	Programmable I/O line 4. Alternative function: TBR_MOSI[1]

Pin#	Pin Name	Pin type	Description
22	PIO[3]	Digital: Bidirectional with programmable strength internal	Programmable I/O line 3.
22	FIO[3]	pull- up/pull-down	Alternative function: TBR_MISO[2]
23	PIO[2]	Digital: Bidirectional with programmable strength internal	Programmable I/O line 2.
23	FIO[2]	pull- up/pull-down	Alternative function: TBR_MISO[3]
24	PIO[1]	Digital: Bidirectional with programmable strength internal pull- up/pull-down	Automatically defaults to RESET# mode when the device is unpowered, or in off modes. Reconfigurable as a PIO after boot.
		Digital: Bidirectional with	Alternative function: Programmable I/O line 1
25	PIO[19]	programmable strength internal	Programmable I/O line 19.
		pull- up/pull-down	Alternative function: PCM_DIN[0]
26	PIO[16]	Digital: Bidirectional with programmable strength internal	Programmable I/O line 16.
	- ( - )	pull- up/pull-down	Alternative function: PCM_CLK
27	PIO[17]	Digital: Bidirectional with programmable strength internal	Programmable I/O line 17.
	110[17]	pull- up/pull-down	Alternative function: PCM_SYNC
28	PIO[18]	Digital: Bidirectional with programmable strength internal	Programmable I/O line 18.
20	FIO[16]	pull- up/pull-down	Alternative function: PCM_DOUT[0]
20	DIO[1E]	Digital: Bidirectional with	Programmable I/O line 15.
29	PIO[15]	programmable strength internal pull- up/pull-down	Alternative function: MCLK_OUT
30	VDD_PADS_1、3	Supply	1.8 V/3.3 V PIO supply.
31	TBR_CLK	Digital: Bidirectional with programmable strength internal pull- up/pull-down	TBR_CLK Alternative function: Programmable I/O line 8.
32	TBR_MISO	Digital: Bidirectional with programmable strength internal pull- up/pull-down	TBR_MISO[0] Alternative function: Programmable I/O line7.
33	TBR_MOS	Digital: Bidirectional with programmable strength internal pull- up/pull-down	TBR_MOSI[0] Alternative function: Programmable I/O line6.
34	LED[1]	Analog or digital input/ open drain	General-purpose analog/digital input or open
35	LED[0]	output.  Analog or digital input/ open drain output.	drain LED output.  General-purpose analog/digital input or open drain LED output.
36	SYS_CTRL	Digital input	Typically connected to an ON/OFF push button. Boots device in response to a button press when power is still present from battery and/or charger but software has placed the device in the OFF or DORMANT state. Additionally useable as a digital input in normal operation. No pull. Additional function: PIO[0] input only
37	1V8	Supply	1.8V voltage output
38	GND	Ground	Ground
39	VBAT	Supply	Battery voltage input.
40	VCHG	Supply	Charger input to Bypass regulator.
41	GND	Ground	Ground

Pin#	Pin Name	Pin type	Description	
42	SPKR_N	VDD_AUDIO_HP_ SPKR	Headphone/speaker differential right output, negative.  Alternative function: Differential right line	
43	SPKR_P	VDD_AUDIO_HP_ SPKR	output, negative  Headphone/speaker differential right output, positive.  Alternative function: Differential right line output, positive	
44	SPKL_N	VDD_AUDIO_HP_ SPKL	Headphone/speaker differential left output, negative.  Alternative function: Differential left line output, negative	
45	SPKL_P	VDD_AUDIO_HP_ SPKL	Headphone/speaker differential left output, positive.  Alternative function: Differential left line output, positive	
46	GND	Ground	Ground	
47	MIC2_P	VDD_AUDIO_1V8	Microphone differential 2 input, positive.  Alternative function: Differential audio line input right, positive	
48	MIC2_N	VDD_AUDIO_1V8	Microphone differential 2 input, negative.  Alternative function: Differential audio line input right, negative	
49	MIC1_P	VDD_AUDIO_1V8	Microphone differential 1 input, positive.  Alternative function: Differential audio line input left, positive	
50	MIC1_N	VDD_AUDIO_1V8	Microphone differential 1 input, negative.  Alternative function: Differential audio line input left, negative	
51	PIO[20]	Digital: Bidirectional with programmable strength internal pull- up/pull-down	Programmable I/O line 20.  Alternative function: PCM_DOUT[1]	
52	PIO[21]	Digital: Bidirectional with programmable strength internal pull- up/pull-down	Programmable I/O line 21. Alternative function: PCM_DOUT[2]	
53	MIC_BIAS	VDD_AUDIO_1V8	Mic bias output.	
54	GND	Ground	Ground	
55	BT_RF	VDD_BT_RADIO	Bluetooth transmit/receive.	
56	GND	Ground	Ground	
57	NC	NC	NC	
58	NC	NC	NC	
59	NC	NC	NC	
60	NC	NC	NC	

# 8 Reference application circuit



Notice: for reference only, please design the circuit according to the actual application

### 9 Electrical Characteristics

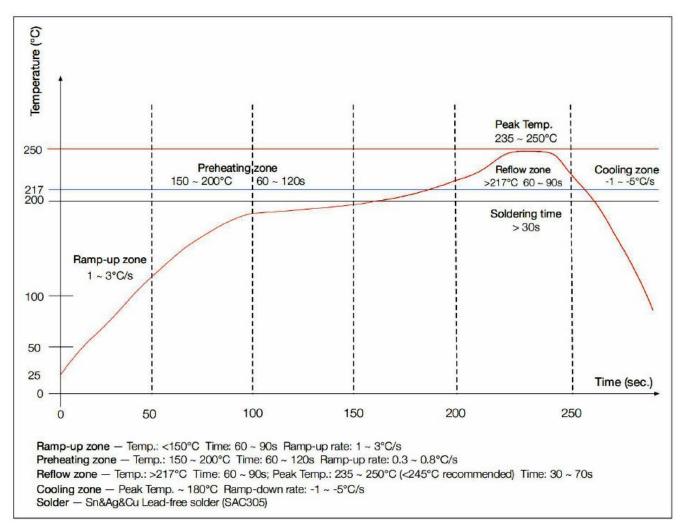
#### 9.1 Absolute Maximum Ratings

Rating	Minimum	Maximum
Storage temperature	-40°C	+85℃

### 9.2 Recommended Operating Conditions

Operating Condition	Minimum	Maximum
Operating temperature range	-40℃	+85℃
Supply voltage: VBAT	+2.8V	+4.3V

## 10 Recommended reflow temperature profile



The module Must go through 100°C baking for at least 12 hours before SMT AND IR reflow process!

#### IMPORTANT NOTICE

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